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Exploring the Influence of Channel Doping Concentration on Short Channel Effects in Nanoscale Double-Gate FinFETs: A Comparative Study

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Abstract

This work investigates the impact of channel doping concentration on short channel effects (SCEs) in different semiconductor materials using FinFETs. The work examines Gallium Arsenide (GaAs), Gallium Antimonide (GaSb), Gallium Nitride (GaN), and Silicon (Si) FinFETs in the PADRE simulator environment which is a powerful component from Multigate Field Effect Transistor (MUGFET) tool readily available at nanoHUB.org, analyzing performance metrics such as Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Threshold Voltage roll-off, transconductance as well as on-current. It is found that GaAs-FinFET exhibits lowest DIBL of 3.63 mV/V at low channel doping concentration, lowest SS of 64.37 mV/V at high channel doping concentration, and highest on-current of 2×10^{-4} *A/μm at low doping concentration, whereas GaN-FinFET exhibits highest transconductance of* 1×10^{-8} *S/μm at low channel doping concentration. However, GaSb FinFET displays lowest threshold voltage of 0.48 V at low doping concentration. The work concludes that low channel doping concentration plays a pivotal role in mitigating short channel effects leading to enhanced operational performance of FinFET devices. This finding provides valuable insight into improving FinFET design and channel material selection for a variety of semiconductor applications.*

1.0. Introduction

Nanoscience and its associated technology has recently seen widespread adoption in multidisciplinary research, especially in the last two decades. In nanotechnology, low-dimensional materials are characterized by their diverse structural configurations, such as nanowires, nanorods, nanophotolithography, nanotubes, and nanocrystalline films [1]. As a result of persistent miniaturization of MOS (Metal Oxide Semiconductor) devices, it is easy to enhance transistor density and performance aggressively. This enables optimal chip functionality at high speeds [2]. Scaling causes traditional MOSFETs to exhibit common negative effects such as DIBL, threshold voltage reduction, and punch-through. These detrimental consequences that are collectively referred to as Short Channel Effects (SCEs) [3]. As a practical example of the multi-gate MOSFET structure, FinFET has emerged as the leading contender for mitigating short-channel effects while adhering to the ITRS roadmap's scaling requirements [4]. High-performance MOSFETs are currently made of strained Si, and increased strain aids in scaling. The advent of higher mobility materials like GaAs and GaSb, along with innovative structures and strains, might even outperform heavily strained Si on the nanoscale in the near future [5].

A number of research works have been conducted to explore the implications of short channel effects (SCE) on finFET devices. In [6], the authors proposed an analytical compact model that can be used to determine the V_{th} of dual gate and triple gate FinFETs. The precision of the model was evaluated by contrasting its predictions with those produced by a Simulator for numerical devices across channel lengths, fin heights, and fin widths. According to the study, the proposed threshold voltage model yields highly accurate predictions, based on a comparison to numerical simulations. In [7], a range of key parameters were assessed to determine how high-k dielectric materials affect FinFET performance. High-k dielectric materials were observed to substantially mitigate issues associated with short channel effects and leakage current when incorporated into the system.
In [8], the performance of strained-Si channel nano-scale transistors and In0.75Ga0.25As III-V semiconductors was compared. They had the same configuration and size. The authors found that performance of In0.75Ga0.25As FETs was not better than that of their strained-Si equivalents. Mustafa et al. studied in [2] the sensitivity of threshold voltage to metal gate work function in double gate FinFET structures, with a focus on evaluating the device's short channel performance. MuGFET's PADRE simulator, based on drift-diffusion theory, was used to simulate the device. Using carefully adjusted metal gate work-functions, they demonstrated that SS and DIBL in FinFETs could be effectively controlled and improved. An analysis of the short channel effects in FinFET structures was conducted in [4] using Si, GaAs, GaSb, and GaN channel materials. The authors examined short channel effects, including DIBL, SS, and threshold voltage roll-off effects. In [1], the impact of channel length reduction and doping variation on multigate FinFETs was studied. The authors demonstrated that variation in gate length and doping concentration directly affect the key electrical parameters of FinFET structures. However, comparative study with regard to the influence of channel doping concentration which is critical for optimizing FinFET performance need to be undertaken.

The study seeks to conduct a comparative analysis of how variations in channel doping concentration influences SCEs in nanoscale double FinFETs employing GaAs, GaSb, GaN, and Si channel materials. The research will be carried out using PADRE simulator, an important simulation software from MUGFET tool. The SCEs under investigation include DIBL, SS, and threshold voltage roll-off as well as performance metrics such as transconductance and on-current. This knowledge can lead to the creation of innovative transistor architectures and materials with enhanced performance and reduced short channel effects.

1.1 Device Structure

Figure 1 illustrates a 2-dimensional FinFET structure used in the current simulation. The device has crucial parts such as source, drain, gate length (also called channel length), and channel width (also called fin width or fin thickness). There is an oxide with oxide thickness T_{ox1} and T_{ox2} placed on top surface of the fin on each side wall [11].

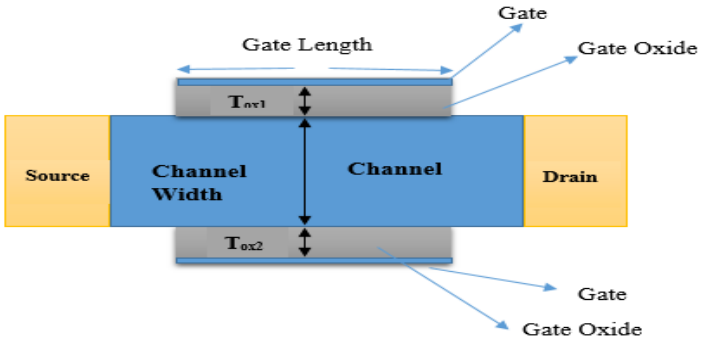

Figure 1. Two-Dimensional FinFET Structure [10]

2.0. Method

The device was simulated using PADRE simulator from MUGFET tool. We investigated the effect of channel doping concentration on short channel effects (SCEs) in different semiconductor materials using FinFETs. In particular, we examined GaAs, GaSb, GaN, and Si FinFETs and analyzed key performance metrics including drain-induced barrier lowering (DIBL), subthreshold swing (SS), threshold voltage roll-off, transconductance, and on-current. Numerous parameters were rigorously studied throughout the modeling of this device construction. In particular, a 45 nm gate length, a 2.5 nm oxide thickness, and constant channel width of 10 nm were used. In the simulation, a range of channel doping concentrations from 1×10^{16} cm^{-3} to 1×10^{18} cm^{-3} were investigated. The drain/source doping was held constant at 1×10^{19} cm^{-3} throughout. Moreover, drain biases of 0.05 V and 1 V were used, and gate bias was systematically changed from 0 V to 1 V. Table 1 gives a comprehensive overview of the aforementioned variables.

Table 1. Simulation Parameter Specifications

Parameter	Value
Gate Length	45 nm
Oxide Thickness	2.5 nm
Channel Width	10 nm
Channel Doping Concentration	(1×10^{16}, 1×10^{17} , 1×10^{18}) cm^{-3}
Source/Drain Doping Concentration	1×10^{19} cm^{-3}
Drain Bias	0.05 V, 1.0 V
Gate Bias	0.0 V to 1.0 V

3.0. Results and Discussion

Presented in this section are the findings of an investigation into the effect of channel doping concentration on FinFET short channel effects. Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), as well as variations in Threshold Voltage were examined. Measurements of transconductance and on-current for these defined channel materials are also included in the results.

3.2. Channel Doping Concentration Versus DIBL

The difference in threshold voltage that occurs when the drain voltage is raised from 0.01 V to 0.05 V is termed as Drain Induced Barrier Lowering (DIBL). The DIBL value can be calculated using [12]:

$$DIBL(\frac{mV}{V}) = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad (1)$$

Where V_{TH} is denotes threshold voltage and V_{DS} denotes drain-source voltage.
Figure 2 depicts how channel doping concentration affects drain-induced barrier lowering (DIBL). The findings show that across the GaAs, GaSb, GaN, and Si FinFETs examined, DIBL increases in a consistent manner with the rise in the channel doping concentration. Notably, when the channel doping concentration is adjusted to 1×10^{16} cm^{-3}, the lowest DIBL value of 3.63 mV/V was obtained using GaAs-finFET, showing its superiority compared to the remaining FinFETs under consideration. This suggests that channel doping engineering and optimization are crucial for FinFET devices. Lowering channel doping concentration can help mitigate DIBL and improve device performance and scalability. Reduced leakage current, greater on-current, better noise margins, scaling compatibility, and increased energy efficiency are just a few of the benefits that lower DIBL in FinFETs could offer. These benefits improve the device's overall functionality and performance.

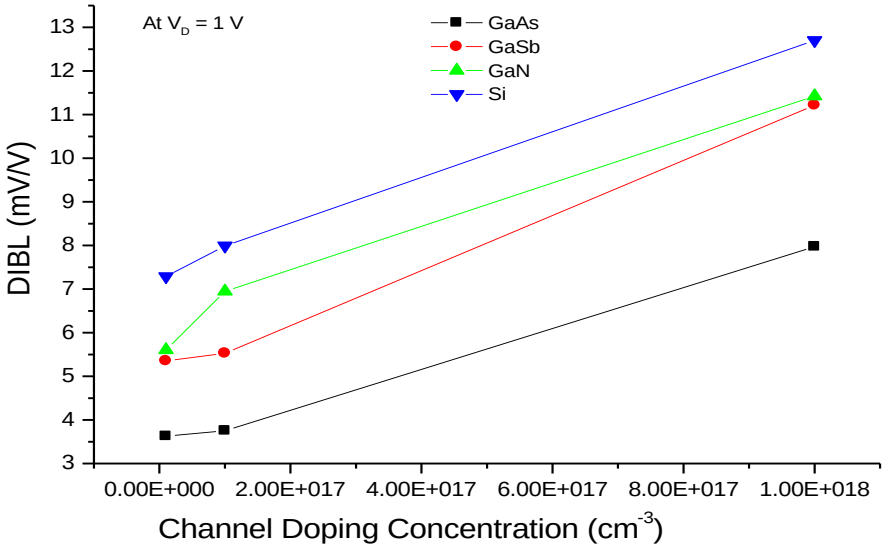

Figure 2. DIBL Vs Channel Doping Concentration

3.3. Channel Doping Concentration Vs Subthreshold Swing

For a Multigate Field Effect Transistor, the SS parameter typically has a value of 60 mV/dec. The SS can be represented by the formula [13]:

$$SS\ (mV/\ dec) = \frac{d\ V_{GS}}{d\ (log_{10}\ I_{DS}} \quad (2)$$

Where V_{Gs} denotes gate-source voltage and I_{DS} denotes drain-source current.
As shown in Figure 3, FinFETs made of GaAs, GaSb, GaN, and Si all have different subthreshold swings depending on the channel doping concentration. It can be seen from the

figure that subthreshold swing decreases in GaAs, GaSb, and Si FinFETs as channel doping concentration increases. This suggests that pathway towards designing more efficient and high-performance FinFET devices. A determination of the optimal channel doping concentration for GaAs-FinFETs reveals that this concentration is characterized by the lowest subthreshold swing of 64.37 mV/dec. This study implies that the subthreshold leakage current, which contributes to the total leakage current in GaAs, GaSb, and Si FinFETs, reduces as the channel doping concentration rises. However, as seen in the graph, with GaN-FinFETs, the subthreshold swing rises as the channel doping concentration does.

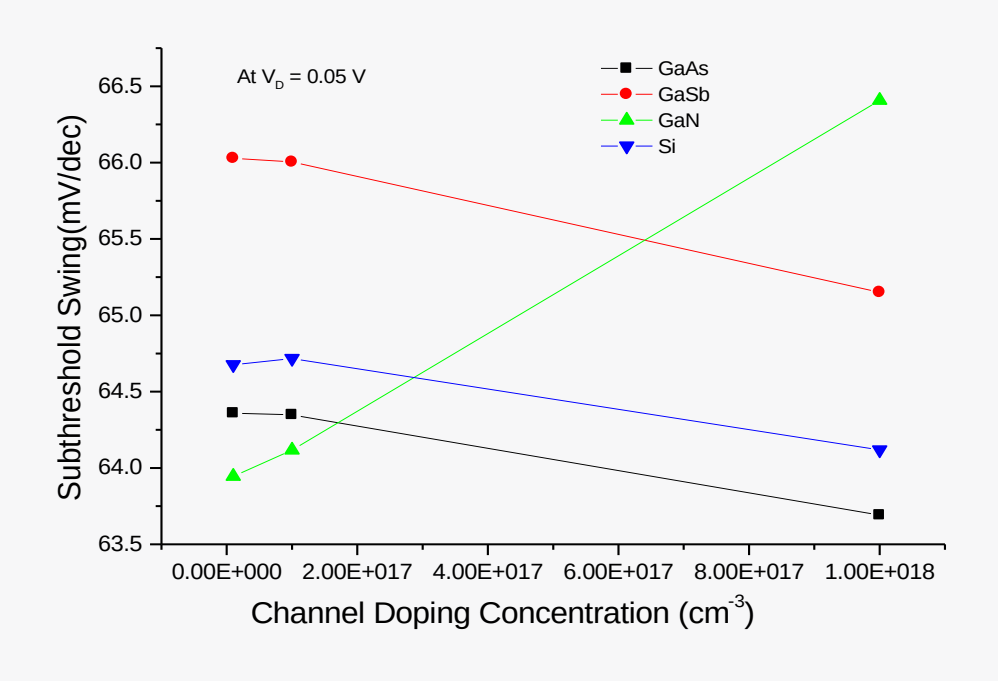

Figure 3. Subthreshold Swing Vs Channel Doping Concentration

3.4. Channel Doping Concentration Versus Threshold Voltage

Threshold voltage is the lowest gate voltage needed to offer a conduction route between the source and drain [14]. The threshold voltage of a FinFET device can be determined using [11]:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \quad (3)$$

Where Q_{SS} denotes gate dielectric charge, C_{ox} is the capacitance in the gate, Q_D is the depletion charge in the channel, f_{ms} denotes metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential, and V_{in} is the additional surface potential to $2f_f$ that is required for ultrathin body devices to cause enough inversion charges in to the channel region of the transistor to reach threshold point.

The effect of different channel doping concentrations on the threshold voltage in FinFETs using channel materials made of GaAs, GaSb, GaN, and Si is shown in Figure 4. The trend suggests that as the channel doping concentration increases, threshold voltage in these devices similarly rises. The four FinFETs have low threshold voltages at channel doping concentrations of 1 1 × 10^{16} cm^{-3}, with GaSb-FinFETs having the lowest threshold voltages of 0.48 V at this concentration. It's important to note that the choice of threshold voltage in FinFETs depends on the specific application and design requirements. In order to maximize power efficiency and performance, low Vth FinFETs are increasingly often employed in contemporary integrated

circuits. This finding provides insights into optimizing transistor characteristics for low-power, high-reliability and process-compatible designs.

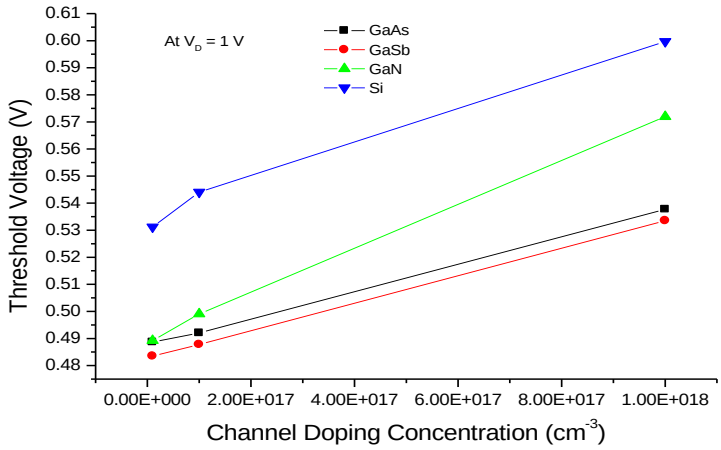

Figure 4. Threshold Voltage Vs Channel Doping Concentration

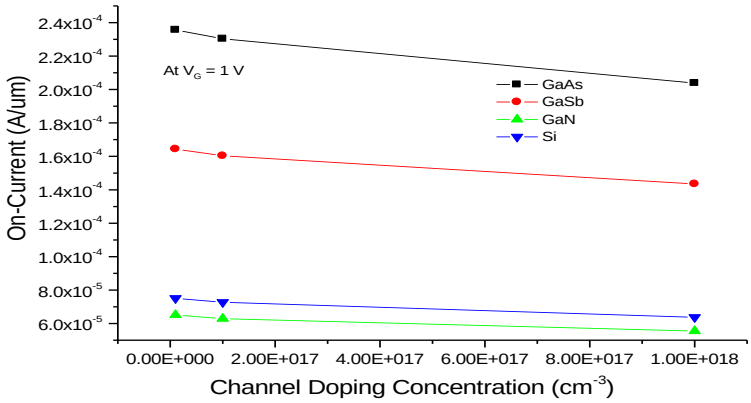

Figure 5. On-Current Vs Channel Doping Concentration

3.2.Doping Concentration Versus Drive Current

Figure 5 shows how drive current (on-current) in GaAs, GaSb, GaN, and Si FinFETs is influenced by the channel doping concentration. The graph demonstrates that as the channel doping concentration increases, the drive current drops in all the four FinFETs. Lower on-current can lead to reduced device performance in terms of speed and switching characteristics. This may impact the overall functionality of the device especially in high-performance computing or data processing applications where fast operation is essential. Notably, compared to the other three FinFETs, the GaAs-FinFET demonstrates a substantially greater on-current of 2×10^{-4} A/μm at the channel doping concentration of 1×10^{16} cm^{-3}. Increased on-current in FinFETs has a number of benefits, including higher noise margins, lower heat production, improved performance, and increased energy efficiency.

3.3. Channel Doping Concentration Versus Transconductance

The transconductance is a parameter that measures how the drain current varies in response to changes in the gate-source voltage while keeping the drain-source voltage unchanged. This parameter can be calculated using [9]:

$$g_m = \frac{dI_D}{dV_{GS}} \quad (4)$$

Where I_D represents the drain current and V_{GS} represents the gate-source voltage

The influence of channel doping concentration on transconductance in FinFETs using GaAs, GaSb, GaN, and Si channel materials is shown in Figure 6. The graphic clearly shows that transconductance in these FinFET devices diminishes as channel doping concentration increases. Transistor with lower transconductance may exhibit slower response times, especially in high frequency applications. This can affect the speed and accuracy signal processing, leading to potential performance limitations in circuits such as amplifiers, filters and oscillators. GaN-FinFET, in particular, stands out with a much greater transconductance of 1×10^{-8} S/μm at the channel doping concentration of 1×10^{16} cm^{-3}, demonstrating its better performance compared to the other three FinFET devices at this concentration.

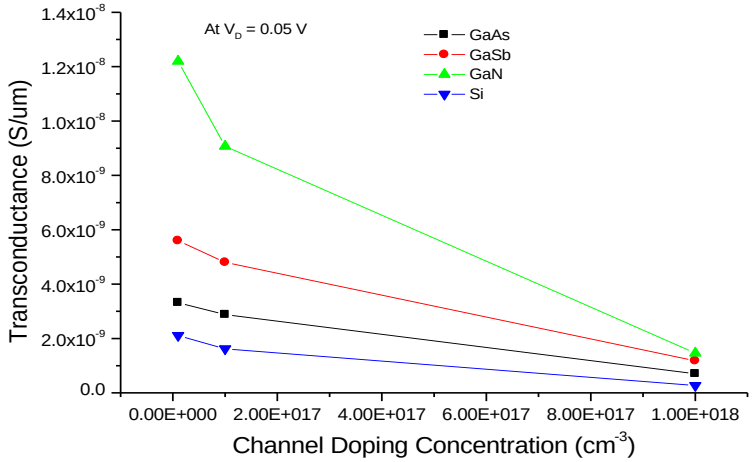

Figure 6. Transconductance Vs Channel Doping Concentration

4. Conclusion

In conclusion, this work examined the impact of channel doping concentration on SCEs in FinFETs utilizing various channel materials, which include GaAs, GaSb, GaN, and Si. Through the analysis, distinct performance differences were revealed. It was found that GaAs-FinFETs exhibited superior performance in relation to DIBL at low channel doping concentration, SS at high doping concentration, and on-current at low channel doping concentration, suggesting potential for enhanced device performance. GaSb demonstrated the lowest threshold voltage at low channel doping concentration, making it excellent in terms of operational speed. GaN-FinFET excelled in transconductance at low channel doping concentration, opening up intriguing possibilities for specific applications. It can be concluded that low channel doping concentration plays a pivotal role in mitigating short channel effects leading to enhanced operational performance in FinFET devices. This finding provides valuable insights for optimizing FinFET design and channel material selection across diverse semiconductor applications. Further research can be carried out to explore the possibility of heterogeneously integrating different channel materials within

the same device to leverage the strengths of each material for specific circuit functions, optimizing overall device performance.

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