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Enhancing FinFET Performance: A Comparative Study of Channel Materials and Short Channel Effects

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Abstract

This work investigates how Short Channel Effects (SCEs) in nanoscale Double Gate FinFETs are affected by varying channel material dielectric constants. Gallium Arsenide (GaAs), Gallium Antimonide (GaSb), Gallium Nitride (GaN), and Silicon (Si) are the channel materials that we investigate. Using the PADRE Simulator, we examine significant metrics such as Drain-Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Threshold Voltage (Vth) Roll-off, on-current, and transconductance. The results show that GaN-FinFETs excel in subthreshold swing at lower dielectric constants and transconductance at higher dielectric constants, whereas GaSb-FinFETs exhibit excellent DIBL properties at lower dielectric constants. GaAs-FinFETs perform better than other FinFETs in terms of threshold voltage and on-current at higher dielectric constants. The findings provide valuable guidance on selecting channel materials to get the best FinFET performance. This knowledge can help designers make informed decisions creating leading-edge semiconductor devices.

1. Introduction

In current electronics industry development trends, rigorous shrinking of electronic device size is carried out in pursuit of improved performance and efficiency [1],[2],[3]. The difficulty of minimizing transistor size increases due to the growing number of obstacles as technological nodes continue to get smaller [4],[5]. These obstacles brought about due to transistor downsize are called Short Channel Effects (SCEs) [6],[7]. In order to surmount the constraints that exist and perpetuate the unending pursuit of advancement, the focus of individuals involved in the field of research and engineering has shifted towards exploring alternate architectures of transistors. The FinFET structure, which has gained prominence in recent years, has emerged as a highly promising candidate in the field of semiconductor technology. This is primarily attributed to its notable advantages, including superior gate control and enhanced fabrication compatibility [5],[8],[9],[10]. Investigating the impact of variations in the dielectric constants of channel materials on short channel effects in FinFETs is a crucial study that not only promotes innovation in the field of nano-electronics but also makes a significant contribution to the long-term viability of semiconductor technology as it evolves and advances.

An in-depth review of previously conducted research has provided priceless insight and knowledge, thereby shedding light on the trajectory that has led us to start our current comparative investigation. This is necessary in the endless effort to understand the intricate correlation between the dielectric constants of channels and resulting short channel effects (SCEs) that occur in FinFETs. A simulator for two-dimensional device was used to examine the effects of dielectric materials, such as gate

oxide, on different short channel device characteristics in [11]. Gate stack technology has been demonstrated to reduce the resultant electric field over the channel and improved device performance.

Extensive research has been conducted in [12] with the goal of improving MOSFET performance and expanding CMOS-based technologies. The results showed that compared to other gate dielectric materials, La_2O_3 gate dielectrics among other high-k materials showed significant improvements in transconductance, threshold voltage, decreased short channel effects (SCEs), and overall increased FinFET performance.

In [1], several gate dielectric materials have been used to investigate the electrical properties of double gate Fin-FETs. Significant transconductance was enhanced. The device's leakage current dramatically reduced when the gate dielectric material HfO_2 was used in place of SiO_2. The authors came to the conclusion that Hafnium oxide (HfO_2) performs better in Double Gate FinFETs than other gate dielectric materials such as SiO_2. The SCEs of several materials with high dielectric constants were examined [13]. It was established that Hafnium Oxide, among the dielectric materials examined, exhibited excellent characteristics since its SCEs were lower than those of the other materials. In [14], SiO_2 was swapped out for a high-k dielectric material (HfO_2). The researchers showed that HfO_2 exhibited decreased SCEs, including lower threshold voltage and off-state leakage current compared to traditional SiO_2, indicating that HfO_2 might be selected as an innovative dielectric material that can mitigate SCEs. While there is research on short channel effects in FinFETs and the effects of numerous dielectric materials on device performance, there is no in-depth comparative analysis that specifically examined the impact of different channel material dielectric constants on short channel effects in nanoscale Double Gate FinFETs.

This work aims at exploring the comparative analysis of variation effect of material channel dielectric constants on short channel effects in nanoscale double gate FinFETs using GaAs, GaSb, GaN and Si as channel materials. The performance parameters investigated include DIBL, SS, threshold voltage roll-off, on-current and transconductance.

1.1 Device Structure

Figure 1 depicts a two-dimensional representation of the FinFET device structure utilized in the current simulation study, as well as the different device parameters that were used in the simulation.

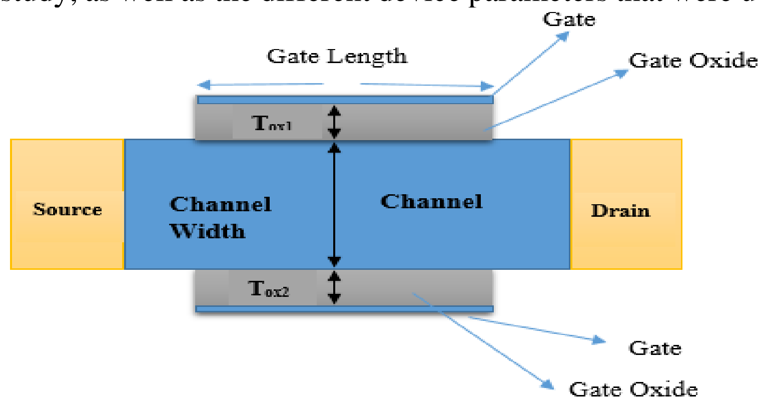

Figure 1. Two-Dimensional Double FinFET [17]

The structure has important parts such the source, drain, gate length (also referred to as channel length), and channel width (also referred to as fin width or fin thickness). Before making the gate contact, the oxide is placed on the top surface of the fin, both on the side walls, and both sides of the side walls. Tox1 and Tox2 stand for the thicknesses of the side wall oxide

2.0. Methodology

We utilized the PADRE Simulator, a component of the Multigate Field Effect Transistors (MuGFET) tool, to perform simulations on our device. This simulator is proficient in generating

informative curves that engineers can employ to characterize the underlying physics of Field Effect Transistors (FETs). Additionally, it provides consistent solutions to the equations of Poisson and drift-diffusion [15][16]. During the simulation, we explored the impact of varying the dielectric constant (ranging from 10 to 45) on four distinct semiconductor materials: GaAs, GaSb, GaN, and Si, each employed as the channel material for the FinFETs. The simulation maintained a constant gate length of 45 nm and a channel width of 10 nm. The oxide thickness was set at 2 nm, while the channel doping concentration was held steady at 1×10^{16} cm^{-3}, and the drain/source at 1×10^{19} cm^{-3}. Our simulations involved drain biases ranging from 0.05 V to 1 V and gate biases spanning from 0 V to 1 V. The parameters are listed in Table 1.

Table 1. Simulation Parameter Specifications

Parameter	Value
Dielectric Constant	(10, 15, 20, 25, 30, 35, 40, 45)
Oxide Thickness	2 nm
Gate Length	45 nm
Channel Width	10 nm
Channel Doping Concentration	1×10^{16} cm^{-3}
Source/Drain Doping Concentration	1×10^{19} cm^{-3}
Drain Bias	0.05 V, 1.0 V
Gate Bias	0V to 1 V

3.0 Results and Discussion

This section presents and discusses the results obtained from our simulations, which is aimed at assessing the performance of FinFET devices under different dielectric constants with GaAs, GaSb, GaN, and Si as channel materials. We evaluated the critical performance metrics, including Drain-Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Threshold Voltage (Vt) Roll-off, on-current, and transconductance, while systematically varying the channel material dielectric constants. The following subsections present our findings for each of these performance parameters.

3.1. Impact of Dielectric Constant Variation on DIBL

The difference in threshold voltage occurs when the drain voltage is raised from 0.01 V to 0.05 V. This is known as Drain Induced Barrier Lowering (DIBL) [17]. The DIBL value can be determined using the equation [18][19]:

$$DIBL(\frac{mV}{V}) = \frac{\Delta V_{TH}}{\Delta V_{DS}} \tag{1}$$

where V_{TH} is denotes threshold voltage and V_{DS} denotes drain-source voltage.

Figure 2 displays the impact of varying channel dielectric constant on the Drain-Induced Barrier Lowering (DIBL) of FinFET devices using GaAs, GaSb, GaN, and Si as channel materials. As depicted in the figure, an increase in the channel dielectric constant results in a consistent and noticeable rise in DIBL for all FinFET devices considered. Of particular note is that GaSb-FinFETs exhibit the lowest DIBL value of 2.66 mV/V, which occurs at a channel dielectric constant of 10, representing its optimal operating point. This is more improved result compared to the one obtained by Kumar et al. [12]. It is clear that GaSb-FinFETs display superior DIBL characteristics compared to the other three FinFET devices across the range of channel dielectric constants tested. This finding suggests that GaSb may hold promise as a channel material for FinFET devices, offering favorable DIBL performance under varying dielectric conditions.

3.2. Impact of Channel Dielectric Constant Variation on SS

The primary factor in determining the leakage current, holding time in dynamic circuits. For a Multigate Field Effect Transistor, the SS parameter typically has a value of 60 mV/dec. The SS can be represented by the formula [16][17]:

$$SS\ (mV/\ dec) = \frac{d\ V_{GS}}{d\ (log_{10}\ I_{DS}} \tag{2}$$

where V_{GS} denotes gate-source voltage and I_{DS} denotes drain-source current.
Figure 3 gives an in-depth investigation of how adjustments in the channel dielectric constant affect the subthreshold swing in GaAs, GaSb, GaN, and Si FinFETs. One important finding is that the subthreshold swing characteristics of GaAs, GaSb, and Si FinFETs are nearly identical when the channel dielectric constant is between 10 and 15, as well as between 30 and 35. This resemblance shows that, within these specified dielectric constant values, both materials may be utilized interchangeably in some applications with no discernible changes in subthreshold swing performance. This information might be useful for engineers and designers looking to select the best materials for their unique device requirements. Furthermore, while operating within the stated dielectric value ranges, the subthreshold swing continuously demonstrates a linear rise with an increase in the channel dielectric constant. The need of carefully changing the channel dielectric constant to enhance subthreshold swing and overall device performance is shown by this linear relationship. Interestingly, there is a significant variability in subthreshold swing values when the channel dielectric constant falls between 15 and 30. Furthermore, it's important to note that when the channel dielectric constant is adjusted to 10, GaN-FinFETs perform better than the other three channel materials as it has the lowest SS value of 63.98 mV/dec. The SS characteristics obtained are excellent compared to the ones obtained by Kailasam et al. [1] and Kumar et al. [12]. The benefits of employing GaN in FinFET technology are highlighted by this result, especially in applications where a low subthreshold swing is essential, such high-performance integrated circuits.

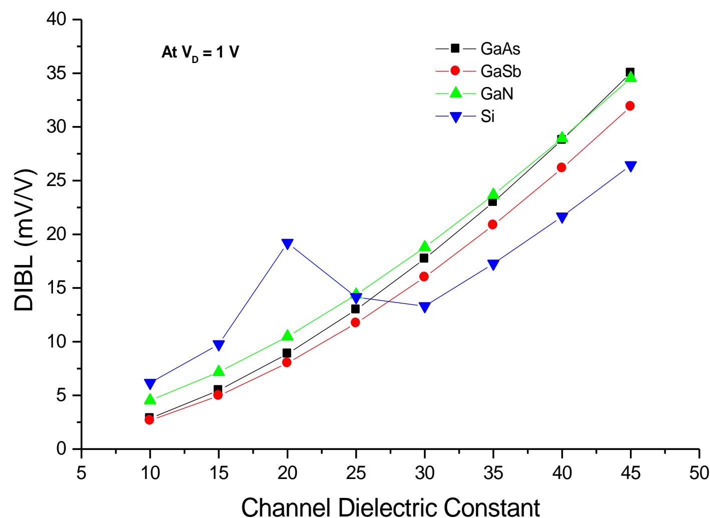

Figure 2. DIBL Vs Channel Dielectric Constant

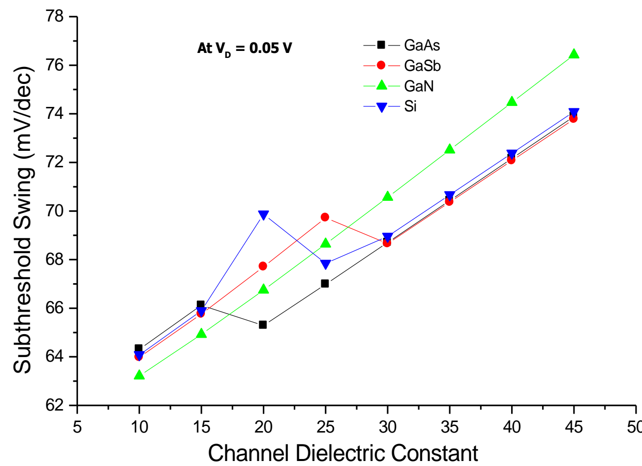

Figure 3. Subthreshold Swing Vs Channel Dielectric Constant

3.3 Impact of Channel Dielectric Constant Variation on Threshold Voltage

Evaluating a device's threshold voltage is an important step in establishing its potential as a viable channel material for switching applications. The threshold voltage is the least gate voltage needed to provide a conduction route between the source and the drain [20]. The threshold voltage of a fin field-effect transistor (FinFET) device can be determined using [19]:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \quad (3)$$

where Q_{SS} denotes charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, f_{ms} denotes metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential.

The graph in Figure 4 depicts the effect of altering channel dielectric constants on short channel effects in GaAs, GaSb, GaN, and Si FinFETs. As the channel dielectric constant is raised, the data in the figure clearly show an almost linear drop in the threshold voltage. Notably, when the Si-FinFET is considered, the threshold voltage shows a noticeable fluctuation within the dielectric constant range of 15 to 30. On the other hand, GaAs-FinFET outperformed the other three FinFETs as it displayed lowest threshold voltage of 0.414 V at the dielectric constant of 45. A relatively similar value was obtained by Kumar et al [12]. The decreased threshold voltage characteristics of GaAs-finFET provides a significant improvement in operational performance. This enhancement has a wider range of benefits, such as higher processing speed, increased energy efficiency, and improved overall functioning [1],[21].

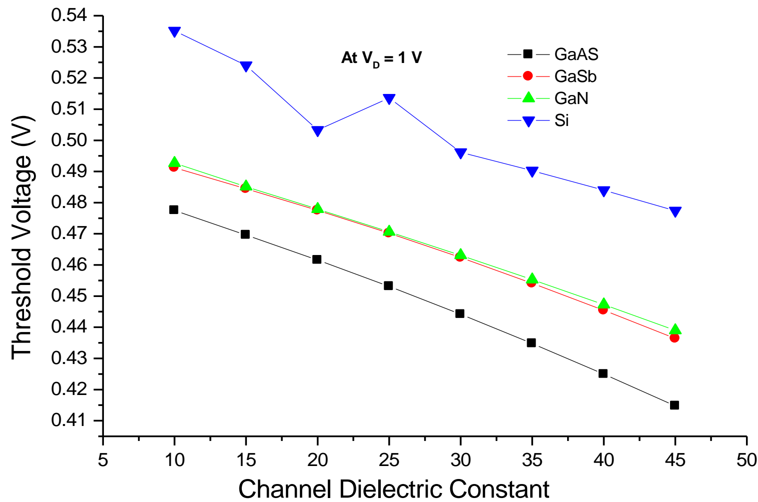

Figure 4. Threshold Voltage Vs Channel Dielectric Constant

3.3.Impact of Dielectric Constant Variation on Drive Current

Figure 5 presents the impact of channel dielectric variation on the drive current of GaAs, GaSb, GaN and Si FinFET. It can be observed that GaN and Si FinFETs maintained relatively constant on-current across the channel dielectric constants under consideration. Furthermore, On-current increases with increase in the channel dielectric constant for GaAs and GaSb FinFETs. GaAs-FinFET performed better in terms of on-current than the other three FinFETs as it showed highest on-current of 2.62×10^{-4} A/um at the channel dielectric constant of 45. This on-current value obtained is higher than that obtained by Anizam et al. [14]. Higher on-current in FinFETs indicates greater device performance, lower power consumption, enhanced integration features, and superior signal quality, making it a critical characteristic in contemporary electronics for both digital and analog applications.

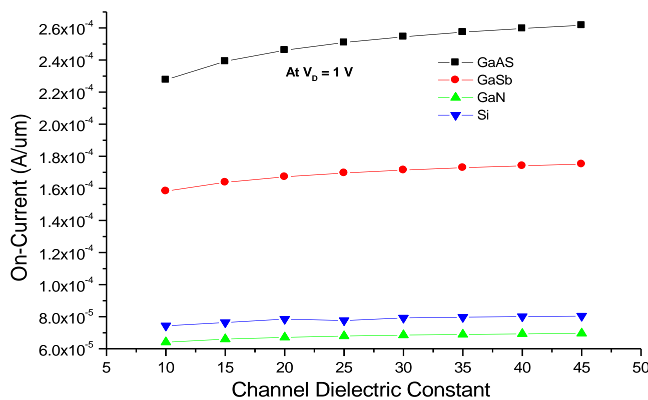

Figure 5. On-Current Vs Channel Dielectric Constant

3.4.Impact of Channel Dielectric Constant Variation on Transconductance

The transconductance measures how the drain current varies in response to changes in the gate-source voltage in the course of keeping the drain-source voltage unchanged. This parameter can be calculated using equation [15]:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{4}$$

where I_D denotes the drain current and V_{GS} denotes the gate-source voltage.

The effect of variations in the channel dielectric constant on the transconductance of FinFETs utilizing various semiconductor materials, such as GaAs, GaSb, GaN, and Si, can be seen in Figure 6. The picture clearly shows that the transconductance of these FinFETs increases as does the channel dielectric constant. Additionally, the comparative investigation illustrated in the figure shows that GaN-based FinFETs outperform the other three FinFETs in terms of transconductance characteristics. Particularly, the GaN-FinFETs in the study showed highest transconductance of 1.11×10^{-7} S/μm at the dielectric constant of 45 indicating their excellent transconductance performance at that point. The potential benefits of using GaN as a semiconductor material in FinFET technology are highlighted by this finding, especially when trying to maximize transconductance for various electronic applications.

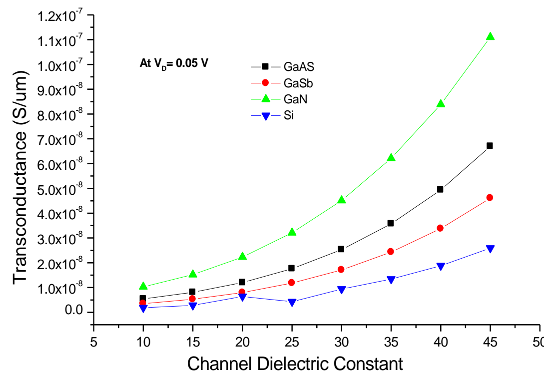

Figure 6. Transconductance Vs Channel Dielectric Constant

4. Conclusion

This comprehensive investigation delved into the intricate interplay of channel material dielectric constants on Short Channel Effects (SCEs) within nanoscale Double Gate FinFETs, employing a diverse array of semiconductor channel materials, including Gallium Arsenide (GaAs), Gallium Antimonide (GaSb), Gallium Nitride (GaN), and Silicon (Si). The study rigorously examined critical performance metrics, encompassing Drain-Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Threshold Voltage (Vt) Roll-off, on-current, and transconductance. The results unveiled distinct material specific strengths: GaN-FinFETs displayed exemplary subthreshold swing at lower dielectric constants and transconductance at higher dielectric constants, GaSb-FinFETs exhibited exceptional DIBL properties at lower dielectric constants, and GaAs-FinFETs excelled in terms of threshold voltage and on-current at higher dielectric constants. These findings offer invaluable guidance to semiconductor device designers in the strategic selection of channel materials to optimize FinFET performance, thereby contributing to advancements in semiconductor technology. Furthermore, the research suggests exciting future directions that involve the exploration of advanced multi-gate transistor devices like nanosheet transistors and the examination of how variations in channel material dielectric constants impact performance and scalability, promising further innovation in the field.

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