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QCA Based Design of Reversible Parity Generator and Parity Checker Circuits for Telecommunication

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Abstract

Quantum-dot cellular automation (QCA) is a transistor-free technology used to implement nanoscale circuit designs. When compared to the widely used complementary metal oxide semiconductor (CMOS) technology, QCA circuits are faster, denser, and use less energy. It has some advantages in reversible logic, including its small size and low power dissipation. In this work, a model of a low-power 3-bit odd parity generator and checker circuit based on a reversible Feynman gate with 23 cells and 40 cells, respectively, is proposed. The proposed reversible odd parity generator and checker circuit can be used in telecommunication systems for bit loss detection and checking. The proposed circuits and the theoretical values are tested using QCA Designer simulator version 2.0.3 to ensure that the circuit works properly, and QCA Designer-E is used to estimate the energy dissipation of the circuits. According to the simulation results, the proposed circuits improve cell counts by 28% for the parity generator, 40% for the parity checker, and 27% for the nano-communication, and occupied area by 72% for the parity generator, 23% for the parity checker, and 14% for the nano-communication.

1. Introduction

The microelectronics industry has seen significant advancements in the speed and size of electronic devices over the last three decades. Moore's law, which states that the number of transistors in a single integrated chip doubles every 18 months [1], has long guided this trend. This trend governs microprocessor development and performance in digital systems. Complementary metal-oxide-semiconductor (CMOS) technology has emerged as a dominant microelectronics technology over the years. The continued and rapid dimensional scaling of CMOS will eventually approach Moore's law's fundamental limit [2]. A shift away from the CMOS paradigm and toward one based on nanostructures could be one way for the microelectronics industry to keep device density growing. Rather than fighting the effects of feature size reduction, these effects are exploited. One nanostructure paradigm (QCA) proposed by [3] is quantum-dot cellular automata. QCA is transistor less that achieves device performance by coupling cells that are suitable for nano-scale binary information on cells through which no current flows [4]. Because QCA technology differs fundamentally from CMOS technology, new and distinct design approaches are required. Exceptional features include extremely high density, fast operation speed at tetra-hertz frequency range, and ultra-low power dissipation. QCA is a promising candidate for designing nanoscale logic circuits [5,6]. Energy loss is a major consideration in traditional digital systems. In 1960,

R.Landaurer demonstrated energy dissipation as a result of information loss in high-tech circuits and systems built with irreversible hardware. The amount of information lost results in kTln2 joules of energy, according to Landauer's principle, where k = $1.38\times 10^{-23}JK^{-1}$ is the Boltzmann's constant and T is the temperature in Kelvin [7]. The primitive combinational logic circuits dissipate heat energy for every bit of information lost during the operation. This is because, according to the second law of thermodynamics, lost information cannot be recovered using any method. Bennett demonstrated in 1973 that to avoid kTln2 joules of energy dissipation in a circuit, reversible circuits must be used[8]. According to Moore's law, the number of transistors will double every 18 months. As a result, energy-saving devices are very popular. Energy loss in a system is proportional to the number of bits erased during computation [9]. Reversible circuits do not lose information when they are reversed.
In this work a 3 bit parity generator and checker circuit was proposed. The proposed circuits are utilized to design a Nano-communication system. The designs are validated by the QCADesigner version 2.0.3 and QCADesigner-E measures energy dissipation. The proposed structures are compared with the design of [10], the considered performance metrics are cell count, latency, and occupied area.

1.1. Related Works
The detection of errors in a received message is a major factor in the lossless transmission of information in telecommunicati\on systems. The complexity of the telecommunication hardware architecture used to detect errors in received information at the nanoscale is the most challenging aspect in terms of power dissipation and device density. [11], proposes designs for the reversible odd-parity generator and odd-parity checker using QCA-based FG. The proposed QCA circuits have a very low quantum cost and require 72 and 130 cells, respectively, for 3-bit input data. [10], proposed an optimal design of conservative efficient reversible parity logic circuits using QCA, it presents a scalable scheme for implementing an improved model of 3-bit odd-parity-bit, generator, and checker circuits, which require 32 and 67 cells, respectively.The work of [12], Proposed a 4-bit irreversible parity generator, the designed circuit consists of 188 cells and occupies an area of $0.20\mu m^2$. This design is based on a proposed X-OR gate designed with 67 cells and $0.06\mu m^2$. The work of [13], Introduced a 4-bit irreversible even parity generator circuit, the designed circuit consists of 168 cells and a 0.28 μm^2 area. QCA design and implementation of parity generator circuit were proposed by [14], the design is a 4-bit irreversible parity generator circuit with 98 cells and occupies an area of 0.11 μm^2. The work of [15] presents a 4-bit parity generator circuit that required 87 cells and 0.10 μm^2. An -ultra-low power generator circuit has been proposed by [16]. This design has achieved a reduction in the number of used cells and area consumption; it consists of 37 cells and $0.05\mu m^2$.
In this work a new QCA structure of reversible Feynman gate is proposed, the proposed gate is used for designing a new form of 3-bit reversible parity generator and checker circuit which have been testified to design efficient nano-communication architecture for data transmission in telecommunication networks.

1.2 Theoretical Review
A reversible logic gate is an n-input, n-output logic device with one-to-one mapping [17, 18, 19, 20], where the number of inputs equals the number of gates' outputs. For each set of input vectors, this produces a distinct set of output vectors [20, 21]. This prevents information loss, which leads to power dissipation. Fan-out and feedback loops are not permitted in reversible logic. Minimum input constants, a minimum number of reversible gates, and a minimum number of garbage outputs are some characteristics of a reversible logic circuit. However, the Quantum-dot Cellular Automata (QCA) is a cell array in which each cell is made up of quantum dots, which are also thought of as sites located at the square cell's corners [2]. The charge is concentrated in the dots. The cell also contains two mobile electrons that can tunnel between the dots. Because of potential barriers

between cells, electron tunnelling out of the cell is not possible. Due to Coulombic repulsion, two free electrons reside at the cell's corners, always diagonally. Figure 2(a) depicts a four-dot QCA cell with the quantum dot's number (site). Equation 1 is used to calculate the cell's polarization (P) [22].

$$P = \frac{(\rho_1+\rho_3)-(\rho_2+\rho_4)}{\rho_1+\rho_2+\rho_3+\rho_4} \quad (1)$$

The expectation value of the number operator on site (dot) for the ground state eigenfunction (ρ_i) is given by equation (2), where*i* is the quantum dot's number 1, 2, 3, and 4 as shown in Figure 1(a).

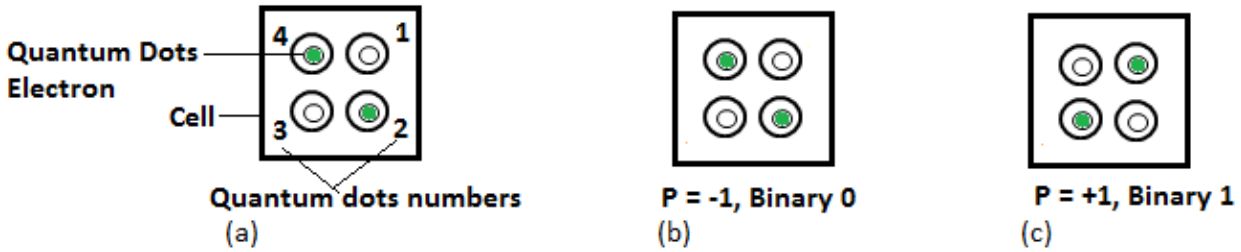


Figure 1: QCA cell (a) schematic (b) with polarization P = "1" (c) with polarization P = "+1". [2]

$$\rho_i = \langle \Psi_o | \hat{\eta}_i | \Psi_o \rangle \quad (2)$$

The ground state of the cell is given by $|\Psi_o\rangle$ and is defined by equation (3) as;

$$|\Psi_o\rangle = \sum_j \Psi_j^0 |\phi_j\rangle \quad (3)$$

Where $|\phi_j\rangle$ is the j[th] vector and $\Psi_j^o$is the coefficient of the basis vector determined by direct diagonalization of the Hamiltonian.

However, the Cell polarization is calculated by locating electrons diagonally. If the electrons are positioned as shown in Figure 2(b), cell polarization P = 1 and are encoded as binary 0 (Logic 0) by equation (1). Similarly, given the location of the electrons in Figure 2(c), the cell polarization P = +1 and is encoded as binary 1 (Logic 1). The information flow in the QCA array is caused by Coulombic coupling between cells. Solving the two-particle Schrodinger equation yields the cell-to-cell response. Cell *j's* polarization is aligned with that of its neighbour cell i in the two-cell system *i* and *j*. In this case, I am regarded as a driver. The Hamiltonian given in equation (4) [23] calculates the two-state models in the N-cell system for single cell *i*.

$$\hat{H} = \begin{bmatrix} -\frac{1}{2}P_j E_{i,j}^k & -\gamma_j \\ -\gamma_j & \frac{1}{2}P_j E_{i,j}^k \end{bmatrix} \quad (4)$$

Equation (5) gives the Kink energy between cells *i* and *j*, where $\gamma_i$is the tunnelling energy and $E_{i,j}^k$ is the tunnelling energy. Cell j's polarization is denoted by Pj. The kink energy E_{kink} can be used to describe the Coulombic interaction between two cells. Kink energy is defined as the difference in electrostatic energies between two cells with opposite polarization and two cells with the same polarization[22].

$$E_{kink}^{i,j} = E_{opposite}^{i,j} - E_{same}^{i,j} \quad (5)$$

where$E_{opposite}^{i,j}$ is the energy between cell *i*&*j* with opposite polarization and $E_{same}^{i,j}$ is the energy between cell *i*&*j* with the same polarization.The electrostatic energy between two cells is used to find the state energy. The electrostatic energy between cells i and j is given by (6).

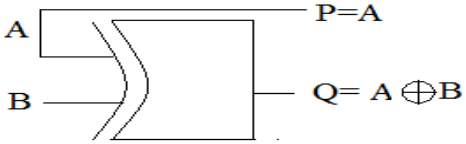
$$E^{i,j} = \frac{1}{4\pi\varepsilon_o\varepsilon_r}\sum_{r=1}^{4}\sum_{m=1}^{4}\frac{q_n^i q_m^j}{|r_n^i - r_m^j|} \quad (6)$$

where ε_o is the permittivity of free space, ε_r is the relative permittivity of a material, q_i^n is the charge in dot n of cell i, q_m^j is the charge in dot m of cell j, r_n^i is the position of the n[th] dot in cell i, r_m^j is the

position of the m[th] dot in cell j, thus $|r_n^i - r_m^j|$ is the distance between the n[th] dot in cell i and the m[th] dot in cell j.

2. Methodology

The Feynman gate with an area of 0.008μm^2, a circuit complexity of 10, and a latency of 0.5 clock cycles are used to design the parity generator and checker circuit, with its input and output having a one-to-one correspondence. The two inputs A and B can be any two variable binary digits to produce two outputs P and Q, which are expressed as P = A and Q = A ⊕ B (A exclusive of B). Figures 2a and b show the proposed reversible Feynman gate schematic logic diagram and QCA layout, respectively.



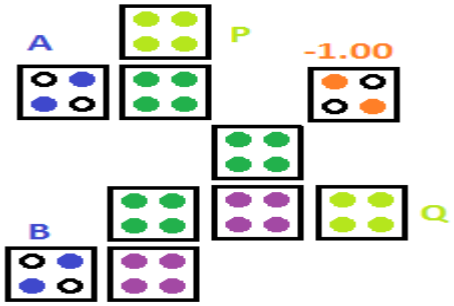


Figure 2: (a) Proposed Feynman gate Logic diagram (b) QCA layout

The truth table of the Feynman gate is described in Table 1

Table 1: Truth table for Feynman gate

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

2.1 Design Procedure/Process

The proposed 3-bit odd parity generator and checker circuit based on a reversible Feynman gate system is divided into two sub-sections for ease of design as follows**:**

1. Reversible odd-parity generator circuit
2. Reversible odd-parity checker circuit

The flow chart in Figure 3 depicts the processes involved in designing the odd parity generator and checker circuit, as well as the integration of the two sub-sections to form the overall system.

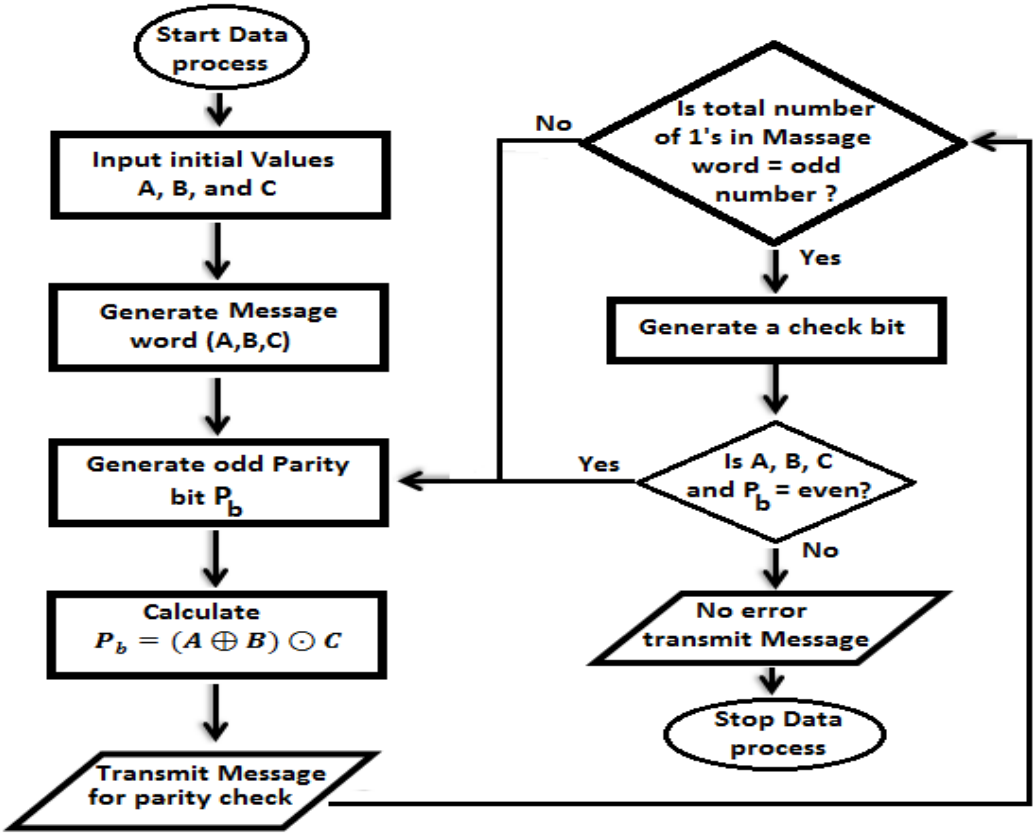


Figure 3: Odd parity generation and checking process

2.1.1 Design of Reversible Odd-Parity Generator Circuit Section

The proposed Feynman gate is cascaded into a 3-bit reversible odd-parity generator, resulting in a 0.032µm^2 area, a circuit complexity of 23, and a latency of 1.5 clock cycles. The logic equation (7) is used to generate an odd parity bit (P_b) and to implement the QCA layout and schematic logic diagram of Figures 4a and b. This system has three input values, A, B, and C, for data communication to ensure that the total number of 1's in the message becomes odd (including P_b).

$$\boldsymbol{P_b = (A \oplus B) \odot C} \quad (7)$$

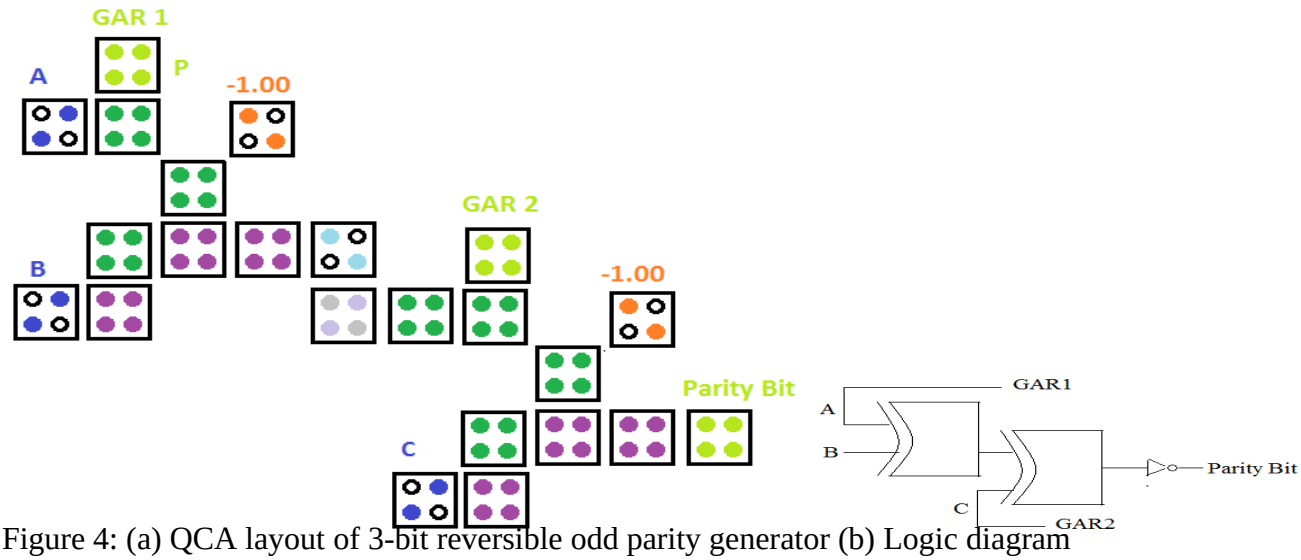


Figure 4: (a) QCA layout of 3-bit reversible odd parity generator (b) Logic diagram

2.1.2 Design of Reversible Odd-Parity Checker Circuit Section

The 3-bit parity checker circuit was designed to check the parity bit that was added to the message word using equation (7) for error detection. The proposed circuit has an area of 0.062μm^2, a circuit complexity of 40 and a latency of 1.5 clock cycles. On the three-bit inputs A, B, and C, a parity check is generated, and the parity bit is expressed using the logic equation (8)

$$\boldsymbol{P_c = (A \oplus B) \odot (C \oplus P_b)} \quad (8)$$

If the message word (three-bit message plus parity bit) is even, an error occurs during transmission. Figures 5a and b show the QCA layout and the schematic logic diagram.

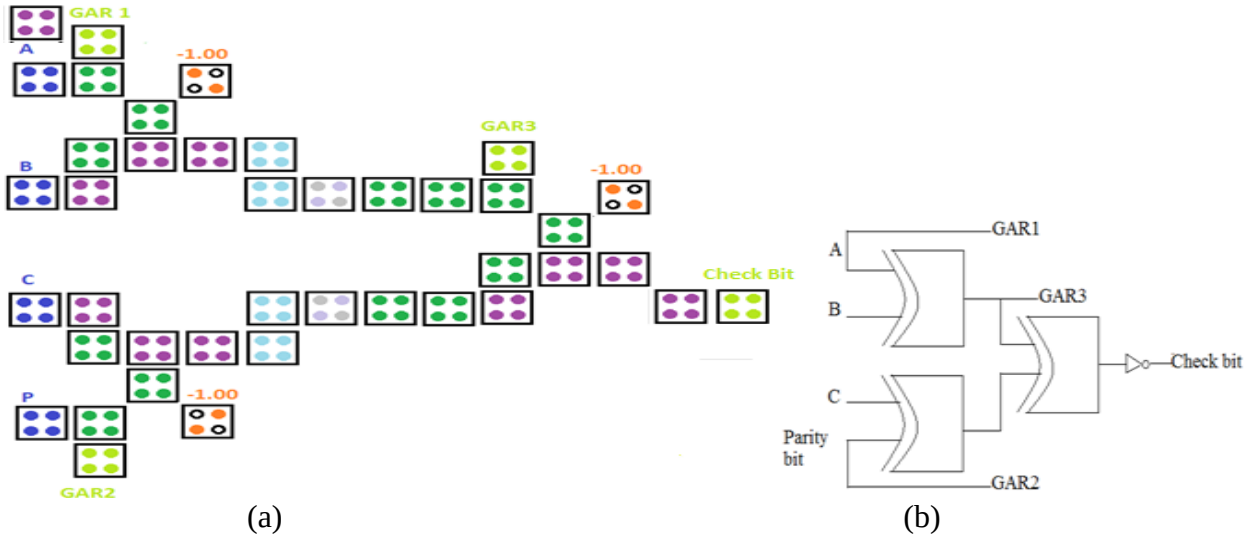


Figure 5: (a) Proposed 3-bit reversible odd parity checker QCA layout (b) Logic diagram

2.1.3 Design Of The General Nano-Communication System Module

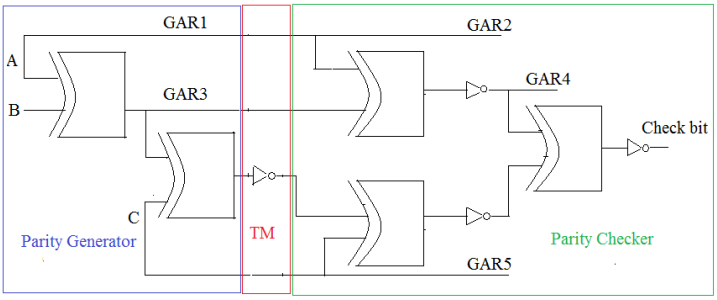
As previously stated, the proposed design of the parity generation and checking system is implemented by cascading the designed parity generation circuit section and the parity checking circuit section through a communication medium to create a complete QCA reversible parity generator and checking telecommunication system. The transmitter (which is the parity generation circuit), transmission medium, and receiver (which is the parity checking circuit) are depicted as the three main components of the nano-communication module in Figure 6. The proposed 3-bit nano-communication system requires 102 cells, occupies 0.13μm^2, and has a delay of 2.0 clock cycles.

Figure 6: Block diagram of the nano-communication module

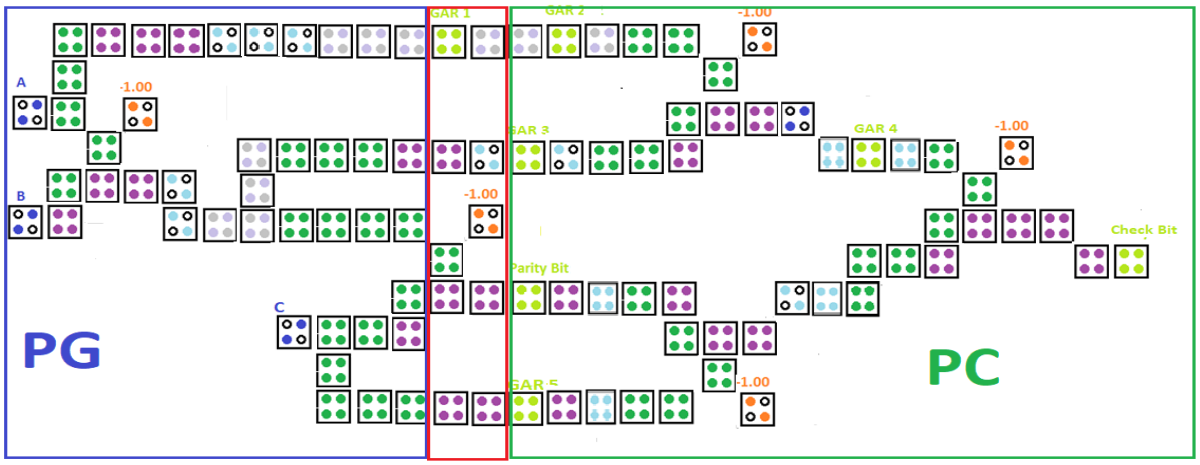
The transmission medium serves as a communication link between the source and destination, the generated transmission bit pattern at the transmitter is sent to the receiver via this medium. The truth table for the nano-communication circuit is presented in Table 2. Figures 6a and b show the QCA layout and the schematic logic diagram of the Nano-communication system.

Table 2: Truth table of Nano-communication system

Parity Generator by the transmitter				Parity Checker				
Message word				Received message by receiver				
A	B	C	Parity Bit	A	B	C	Parity Bit	Check bit
0	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	0	0
0	1	1	1	0	1	1	1	0
1	0	0	0	1	0	0	0	0
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	0	1	0
1	1	1	0	1	1	1	0	0



(a)



(b)

Figure 7: (a) Proposed nano-communication system QCA layout (b) Logic diagram

3. Result and Discussion

The proposed circuits are designed and verified using the QCA-Designer tool version 2.0.3[23]. The default parameters for the simulation are: QCA cell size = 18 nm, diameter of quantum dots = 5 nm, number of samples = 50,000, convergence tolerance = 0.001, radius of effect = 65 nm relative permittivity = 12.9, $clock\ low\ =\ 3.8E^{-23}\ J$, clock $high\ =\ 9.8E^{-22}\ J$, clock amplitude factor = 2.000, layer separation = 11.5 nm and maximum iterations per sample = 100.

3.1 Simulation Result Of The Proposed Reversible Feynman Gate

Figure 8, describes the simulation results of the proposed Feynman gate. It is observed from the simulation results, that when the Inputs are A= 0 and B= 0, the Output becomes P= 0 and Q=0. Similarly, if the Inputs are A= 0 and B=1, Output becomes P= 0 and Q= 1, and the process continues, for other values of the input data these results are in line with the theoretical values shown in Table 1.

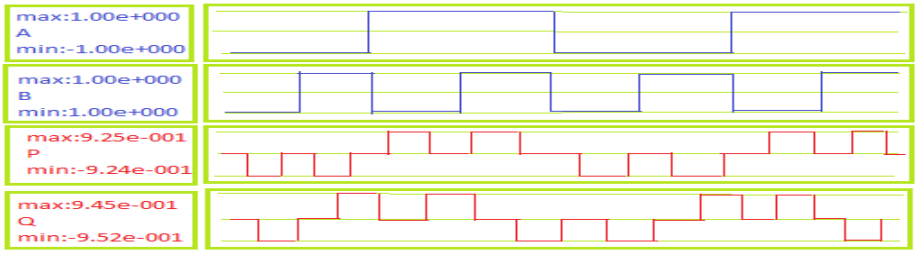


Figure 8: Simulation result of Feynman gate

3.2 Simulation Result Of The Proposed Parity Generator Circuit

The simulation result of the proposed reversible odd-parity generator circuit is shown in Figure 9. The simulation results are tested with the theoretical values shown in Table 2. For inputs A=0, B=0, and C=0, the output will be GAR1=0, GAR2=0, AND P_b=1. When the input values are A=0, B=0, and C=1, the output will be GAR1=0, GAR2=0, AND P_b=0, and the process continues. Therefore the circuit function efficiently.

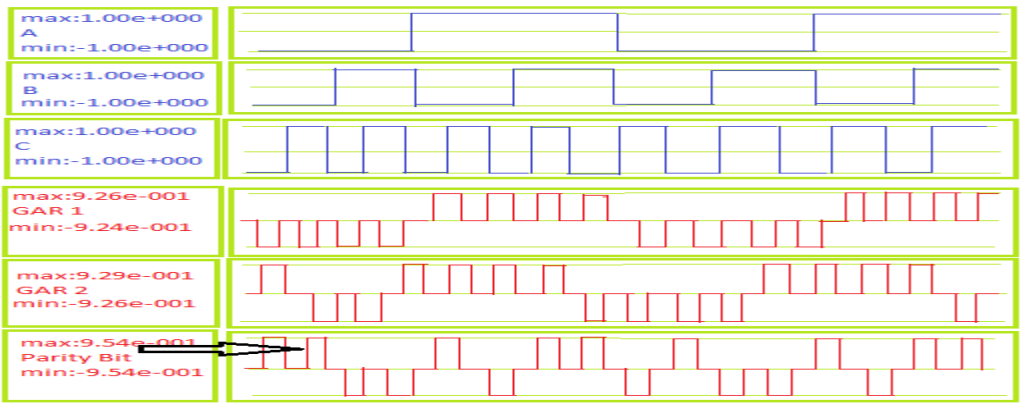


Figure 9: Simulation result of reversible odd Parity Generator

3.3 Simulation Results of The Proposed Parity Checker

Figure 10, describe the simulation results of the proposed reversible odd-parity checker circuit. It is observed from the simulations results, if A= 0, B= 0, C= 0, and Parity bit =0 are taken as inputs and GAR1 = 0, GAR2 = 0,GAR3 =1, and Check bit = 1 are generated as outputs. If the inputs are, A= 0, B= 0, C= 0, and Parity bit =1, then the outputs become GAR1 = 0, GAR2 = 0, GAR3 =0 and Check bit = 0, and the process continues.

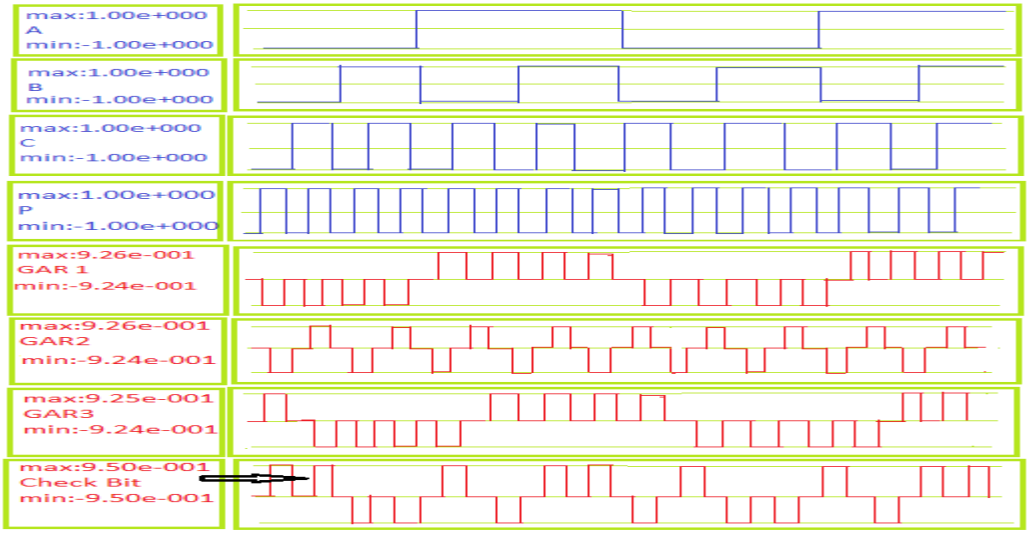


Figure 10: Simulation result of reversible odd Parity checker

3.4 Simulation Result of The Proposed Nano- communication Circuit

The simulation result of the proposed nano-communication circuits is shown in Figures 11. The results are verified with the truth table of the proposed nano-communication circuit shown in Table 2. At the transmitter section, Inputs are labelled as A= 0, B= 0, and C= 0, the outputs become GAR1 = 0, GAR3 = 0, and Parity bit = 1. On the other hand, the outputs become GAR1 = 0, GAR3 = 0, and Parity bit = 0; when inputs are A= 0, B= 0, C= 1. Similarly,when the inputs to the parity checker are taken as A= 0, B= 0, C= 0, and Parity bit = 1, the outputs become GAR2= 0, GAR4 = 1, GAR5 = 1 and Check bit = 0. On the other hand, the outputs turn into GAR2 = 0, GAR4 = 1, GAR5 = 0 and Check bit = 0 when inputs are set at A= 0, B= 0, C= 1 and Parity bit = 0. The verification shows that the communication circuit produces correct outputs.

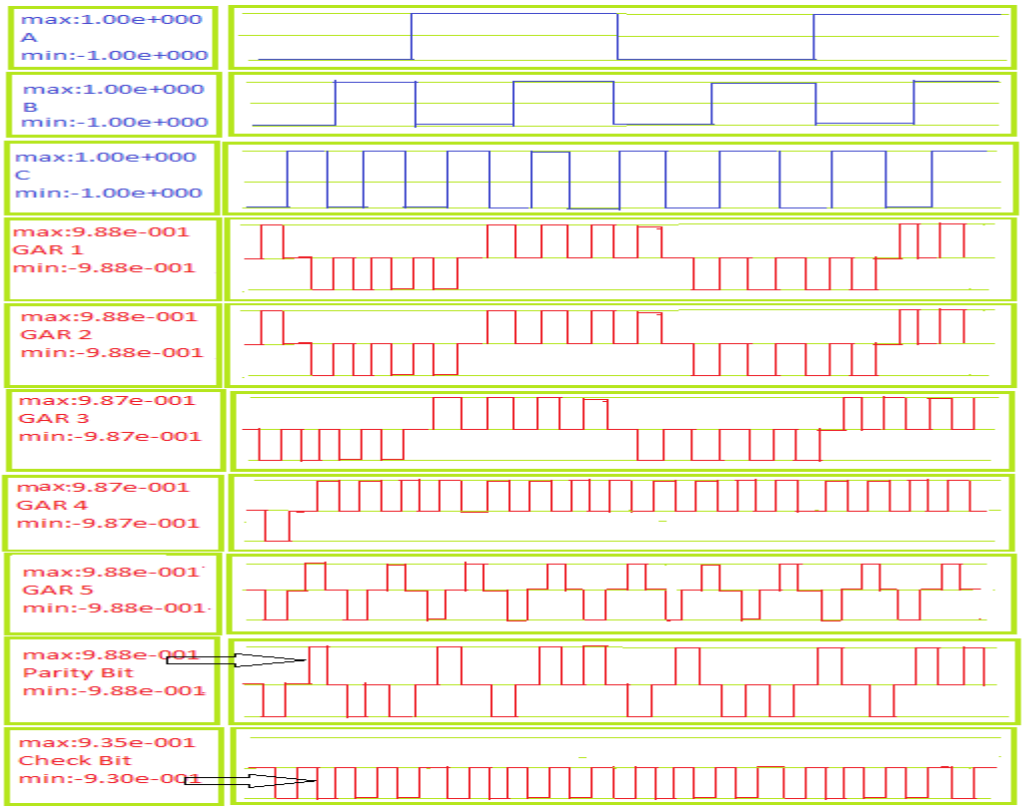


Figure 11: Simulation result of nano-communication system

3.5 Analysis and Comparison of Results

In this section, a comparison of the proposed structures with the existing designs is described. The proposed designs are validated by the QCADesigner version 2.0.3 and QCADesigner-E measures energy dissipation. For comparison, some of the best previous circuits have been selected and compared. The considered performance metrics are cell count, latency, and occupied area.

Cell count is the total number of QCA cells used for designing the proposed circuits. The total area is the product of the number of rows, columns and individual cell areas. Clock latency is showing the design delay and it is calculated by observing the used clocks from input to output. The design complexity of the proposed circuit in terms of the number of QCA cells, total area and clock delays are presented in Table 3 while Table 4 shows a comparison between the complexities of existing and proposed design according to the number of cells, occupied area and delay. According to Table 4, the proposed 3-bit reversible odd parity generator has 23 cells which are reduced by 28.12% compared with the structure of [11]. Also, the occupied area of the proposed parity generator structure is $0.032\mu m^2$, leading to an improvement of 72% compared with the [11] structure. The structure of the proposed reversible parity checker according to Table 6 has 40 cells, that is, improved by 40.29% compared with[11]. The occupied area of the above-mentioned structure is $0.062\mu m^2$, which is improved by 23.45%, in comparison with [11], structure. The proposed reversible nano-communication system has 102 cells that have about 27.14% cell reduction compared with[11]. In addition, with the occupied area of $0.132\mu m^2$compared with the structure of [11], it is improved by 14.83%. According to Table 6, as explained, the proposed structures have made significant improvements compared with [11] structures.

Table 3: Design complexity of the proposed circuit

Proposed QCA circuit	No. Of QCA cells	Total area (μm^2)	Latency
Feynman gate	10	0.008	0.5
Parity generator	23	0.032	1.5
Parity checker	40	0.062	1.5
Nano-communication system	102	0.132	2.0

Table 4: Result Comparison of this work and other Related works.

QCA Circuits	Cell count	Area (μm^2)	Latency
Feynman Gate [24].	53	0.070	1.25
Feynman Gate [25].	34	0.038	0.75
Feynman Gate [11].	43	0.038	0.75
Feynman Gate [10].	16	0.017	0.5
Feynman Gate [26].	11	0.0092	0.5
Proposed Feynman Gate[This work]	10	0.008	0.5
Parity Generator [10].	72	0.078	1.75
Parity Generator [11].	32	0.033	0.75
Proposed Parity Generator[This work]	23	0.032	1.5

Parity checker [10].	130	0.143	2.0
Parity checker [11].	67	0.081	1.0
Proposed Parity checker[This work]	40	0.062	1.5
Nano-communication circuit [10].	293	0.479	2.0
Nano-communication circuit [11].	140	0.155	2.0
Proposed Nano-communication circuit [This work]	102	0.132	2.0

The power consumption of the QCA circuit depends on logical gates used in circuit design [27]. Energy dissipation computing software, QCADesigner-E version 2.2 with default parameters is used to calculate the energy dissipation of the proposed circuits. QCA Designer-E calculates the summation energy for all possible coordinates. There are several energy dissipation components in a QCA circuit such as bath of energy (E_bath), clock energy (E_clk), the energy of a cell (E_io), input energy of a cell (E_in), and output energy of a cell (E_out). E_io, E_out, and E_in are related as shown in Equation 11[28].

.

$$E_{io} = E_{out} - E_{in} \quad (9)$$

The error in energy calculation (E_Error) is given as,

$$E_{Error} = E_{env} - E_{clk} - E_{io} \quad (10)$$

Table 5: Energy dissipation for the proposed circuits

QCA circuits	Total energy Dissipation (eV)	Error (eV)	Average energy dissipation (eV)	Error (eV)
Feynman gate	7.74e-003	-8.23e-004	7.03e-004	-7.48e-005
Parity generator	1.47e-002	-1.52e-003	1.34e-003	-1.39e-004
Parity checker	1.60e-002	-1.56e-003	1.45e-003	-1.42e-004
Nano-communication	2.20e-002	-1.76e-003	2.00e-003	-1.60e-004

The coherence vector simulation engine is used for the calculation of energy dissipation in QCA Designer-E. Default values are selected for the simulation purpose with 500 000 samples. The Euler method with Gauss type clock is taken for the estimation of energy dissipation. The total energy dissipation and average energy dissipation with corresponding errors are computed and presented in Table 5 for all the proposed circuits. Total energy dissipation is the summation of E_bath for all the coordinates while average energy dissipation is the average of E_bath per cycle. Table 5 shows that when the complexity of the circuit is increasing then energy dissipation is also increasing. E_Error is negative because energy transferred to the environment is less as compared to the summation of clock energy and the cell's input-output energy. E_error is also increasing with the increased complexity.

4. Conclusion

In a telecommunication system, error detection and correction in a receiver message are main factors to be taken into consideration. In addition, circuit reversibility in QCA helps designs a lot. In this research, the parity generator and checker circuits and subsequently their nano-communication system is designed reversibly using odd parity bit. . The proposed designs are extensively analyzed and compared with the previous available similar designs by considering a range of performance metrics such as cells count, cell area, and latency. The computational simulation results of the proposed QCA circuits have been authenticated using the QCADesigner tool and energy dissipations have been carried out using QCA Designer-E.

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