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Performance Analysis of Nanoscale Double Gate Ge and GaSb finFETs

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Abstract

This paper explores the performance characteristics of Germanium (Ge) and Gallium Antimonide (GaSb) as potential channel materials for finFET devices. The analysis focuses on key factors such as transconductance, on-current and short channel effects (SCEs) using simulations conducted in the Padre Simulator environment. The results reveal that GaSb-finFET exhibits superior transconductance and on-current as well as reduced short channel effects; drain induced barrier lowering (DIBL) and threshold voltage roll-off compared to Ge-finFET. However, Ge-finFET exhibits better characteristics in terms of subthreshold swing (SS). These findings are particularly important in application where faster switching capabilities are required.

1. Introduction

As we continue to reduce the size of the conventional MOSFETs, achieving excellent performance in semiconductor devices has become more difficult. There will be difficulties if we continue to scale down MOSFETs in the nanoscale regime because of negative effects such as increase in leakage current, drain induced barrier lowering (DIBL), voltage threshold variation and velocity saturation[1][2]. These negative effects are called short channel effects (SCEs).To mitigate the above mentioned effects, it is believed that an alternate structure, such as the Double Gate FinFET (DG-FinFET), can be used to solve the scaling issues, particularly with regard to the device's short channel performance and scalability of nanoscale[3]. The recent focus on FinFET research is due to their many well-known benefits, such as decreased short channel effects[4].
Several studies have been conducted on the short channel effects in fin Field Effect transistors (finFETs). Veshala *et.al* in [5] carried out a research which led to the suppression of leakage current and control of threshold voltage roll-off. Optimization of high performance bulk finFET has been done by researchers in[6]. It has been discovered that the bulk FinFET with bottom spacer can be tuned to outperform all other FinFETs. To improve short channel performance of a finFET another research by[7] has been conducted. The authors reported reduced short channel effects. The impact of downscaling of nano-channel dimensions of Indium Arsenide Fin Feld Effect Transistor (InAs-FinFET) on electrical characteristics of the transistor has been studied in[8]. The authors obtained optimal dimensional parameters' values at scaling factor, K=0.125. In [9], the influence of fin height and width of an n-finFET has been extensively studied. It was proved by the authors that the optimized fin height lies between 50-60 nm.

They also found that the threshold voltage shift by quantum confinement has a steep increase as fin width shrinks to 4 nm. Impact of high-k gate dielectrics on the short channel effects has been studied in[10].They showed that HfO_2 can be considered as a promising candidate that may be used for nanoscale low power applications. Various electrical characteristics of DG finFET have been analyzed at 45 nm by [11]. The authors used different kinds of dielectric materials in search of the better one. They found that TiO_2 enhanced device functionality, improves gate control over the channel, decreases effective leakage current, and provides high amplification values. In [12] the authors studied short channel effects for Silicon (Si), Gallium Arsenide (GaAs), Indium Arsenide (InAs) and Indium Phosphide(InP) as channel materials in nanoscale MOSFET. The authors were able to show that InSb was the best to be used as channel material.

Study of short channel effects for Si, GaSb, GaAs and GaN channel materials has been carried out by [13]. The authors proved that GaN was the worst in terms of immunity against short channel effects. Comparative performance was carried out by [14] between Silicon (Si) and Gallium Nitride (GaN) as channel materials in finFET. GaN was found to have higher performance at higher voltages and higher temperature than Si. However, no comparative analysis has been conducted on the resistance of Ge and GaSb to short channel effects (SCEs) to determine one which is more immune to SCEs that can be a potential channel material in finFET.

The aim of this study is to evaluate the performance of Ge and GaSb channel materials in finFETs, and to identify the material that exhibits superior performance. The study considers various important parameters such as short channel effects, including drain induced barrier lowering (DIBL), sub-threshold swing (SS), and threshold voltage roll-off, as well as drive (on-current) and transconductance. To accomplish this, simulations are conducted on both Ge and GaSb materials in finFETs.

2.0. Methodology

2.1. Device Structure

A 2-D image of the FinFET device structure used in the current simulation work is depicted in Fig. 1, which also specifies the various device parameters used for the simulation investigation.

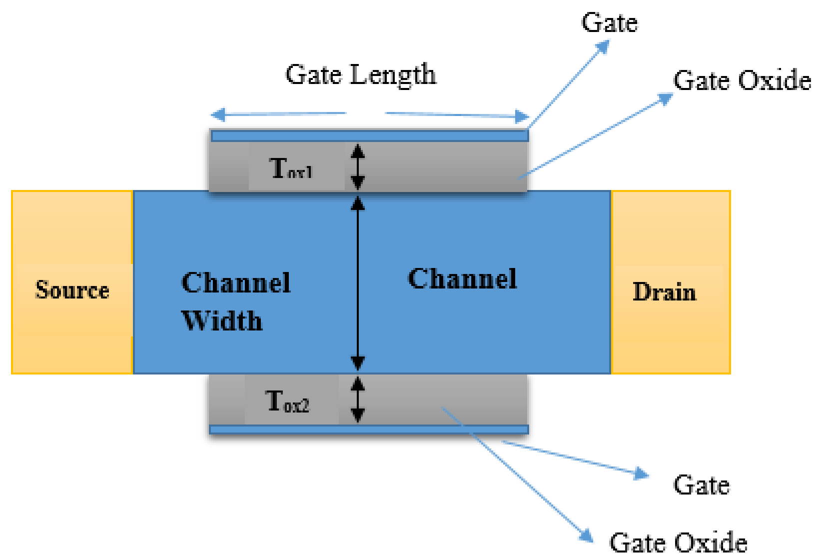

Fig. 1. Two-Dimensional Double Gate FinFET [15]

2.2. Simulation Tool

In this research study, a notable MuGFET tool from nanoHUB.org has been used to simulate the proposed device. MuGFET tool was developed and designed by Purdue University (USA). MuGFET can simulate with either PADRE or PROPHET, both of which were invented by Bell Laboratories. PROPHET is a partial differential equation profiler for one, two, or three dimensions, whereas PADRE is a device-oriented simulator for 2D or 3D devices with any shape. The software may generate valuable characteristic FET curves for engineers, particularly to thoroughly explain the fundamental physics of FETs. It can also provide self-consistent solutions to poison and drift-diffusion equations[16].

2.2.1. Simulation Design

The simulation tool is used to look into the characteristics of finFET using Ge and GaSb as channel materials. The output characteristic curves of the transistor are considered. The device is simulated and evaluated at 300K using the simulation parameters listed in Table 1.

Table 1. Simulation Parameters

Gate Length	45nm
Channel width	10nm
Oxide thickness 1	2nm
Oxide thickness 2	2nm
Initial gate bias	0V
Final gate bias	1V
Initial drain bias	0.05V
Final drain bias	1V
Source extension length	50nm
Drain extension length	50nm
Final drain bias	1V
Band gap for GaSb	0.78 eV
Electron mobility for GaSb	5000 cm^2/V-S
Hole mobility for GaSb	1400 cm^2/V-S
Electron affinity for GaSb	4.06 eV

3. Results and Discussion

This paper compares the results obtained for Ge and GaSb. Transconductance, drain current, threshold voltage, subthreshold swing, drain induced barrier lowering (DIBL) of Ge and GaSb are plotted on various figures. The results are obtained at various values of drain and gate voltages.

3.1.Gate Voltage Variation with Drain Current

Fig. 2 illustrates a graph plotting the drain currents of Ge-finFET and GaSb-finFET for varying gate voltages. Current in GaSb increases as the gate voltage increases. This behavior is also reported in [15]. It is evident from the graph that GaSb-finFET exhibits higher on-current than the Ge-finFET at $V_G = 1.0$ V. Higher on-current in FinFET devices can lead to improved performance, faster switching speeds, enhanced circuit speed, reduced propagation delay, improved power efficiency, better noise margins, and increased design flexibility. These implications make FinFETs desirable for high-performance and power-efficient applications in various fields, including microprocessors,

memory devices, and integrated circuits. It is worth noting that while on-current brings advantages, it also increases power dissipation and heat generation. Therefore, proper thermal management is crucial to ensure the device operates within acceptable temperature limits.

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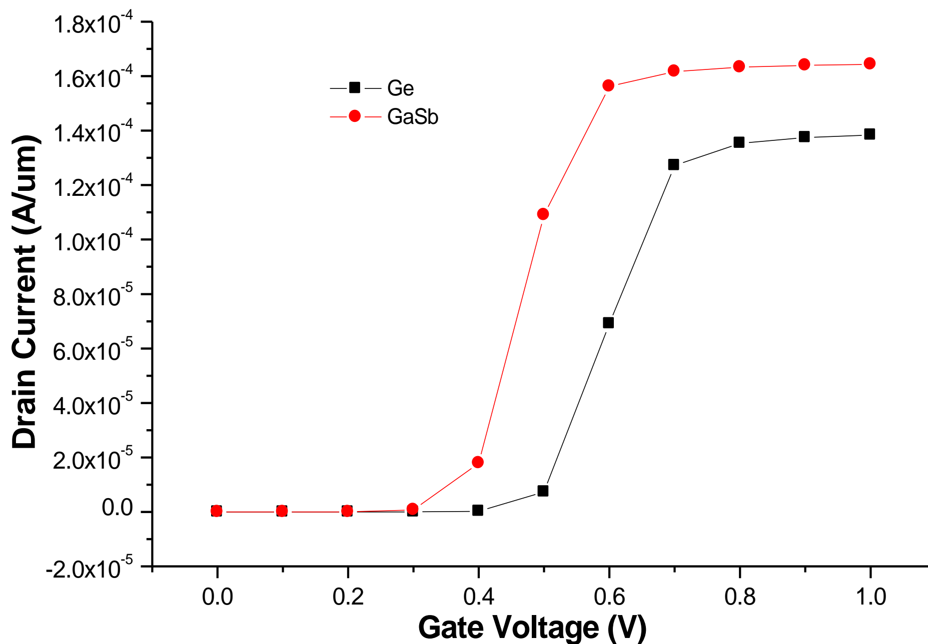

Fig. 2. Gate Voltage Vs Drain Current

3.2. Drain Voltage Variation with Transconductance

The transconductance, g_m quantifies the drain current variation with a gate-source voltage variation while keeping the drain- source voltage constant [15 -16]:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{1}$$

where I_D is the drain current and V_{GS} is the gate-source voltage. Therefore, the value of gm is extracted by taking the derivative of the I_D-V_{GS} curve.
In Fig. 3, the variation of transconductance for Ge-finFET and GaSb-finFET with respect to drain voltage is presented. According to the graph, GaSb-finFET maintains a constant transconductance of 0 S/μm between drain voltages of 0.01V and 0.25V. The transconductance gradually increases with drain voltage and reaches a peak value of 9.11×10^{-4} S/μm at the drain voltage of 0.45 V. In contrast, the transconductance of Ge-finFET starts at 0 S/μm for drain voltages between 0V and 0.38V. It then increases until it reaches a maximum value of 6.2×10^{-4} S/μm at 0.55 V and then

declines at higher drain voltages. Comparing the two, GaSb-finFET has a highest transconductance as compared to Ge-finFET. Higher transconductance in FinFET devices offers advantages such as improved switching performance, higher drive currents, lower power consumption, enhanced noise immunity, and compact design. These benefits contribute to the continued advancement of semiconductor technology, enabling more efficient and powerful finFET devices.

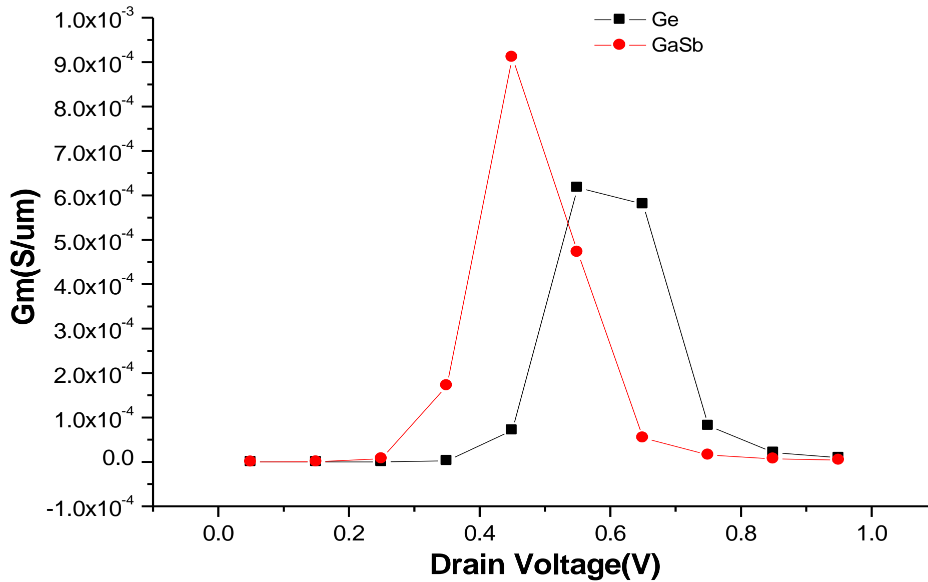

Fig. 3. Drain Voltage Vs Transconductance

3.3.Drain Voltage Versace Threshold Voltage.

Analyzing the threshold voltage of a device is of utmost importance when assessing its suitability as competent channel material for switching purposes [18]. The Threshold voltage is the minimum gate voltage required to set up a conduction path between the source and the drain[2]. The threshold voltage expression in case of a multi-gate field effect transistor (MuGFET) device structure can be expressed as [19]:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \qquad (2)$$

where Q_{SS} represents charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, f_{ms} represents metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential.

As shown in Fig. 4, the threshold voltage for GaSb-finFET is 0.48 V, whereas for Ge-finFET, it is 0.61 V at a drain voltage of 1 V. It is also observed that threshold voltage decreases as the drain voltage increases in both Ge and GaSb-finFETs. This lower threshold voltage for GaSb-finFET results in faster operation [10, 14]. Moreover, the lower threshold voltage aligns with the International Technology Roadmap for Semiconductors (ITRS) 2013 [3]. FinFET devices with a well-optimized threshold voltage can achieve lower power consumption. By carefully adjusting the threshold voltage, the leakage current can be minimized, leading to improved power efficiency. This is particularly important in modern electronic devices where power efficiency is a critical factor.

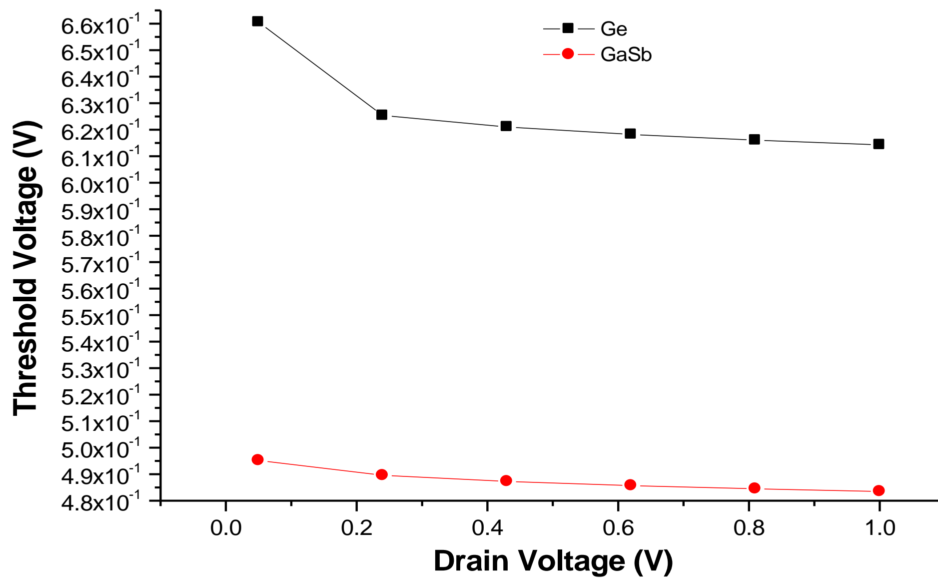

Fig. 4. Drain Voltage Vs Threshold Voltage

3.4.Drain Voltage Variation with Subthreshold Swing

The subthreshold slope is the major parameter for calculating the leakage current. Furthermore, SS is calculated as in [16]:

$$SS\ (mV/\ dec) = \frac{d\ V_{GS}}{d\ (log_{10}\ I_{DS}} \tag{3}$$

Where V_{GS} is the gate-source voltage and I_{DS} is the drain-source current.

A typical value for the SS parameter of a MuGFET is 60 mV /decade, (i.e., a 60 mV change in gate voltage brings about a tenfold change in drain current) [17].
Fig. 5 shows a comparison of the subthreshold swing between Ge-finFET and GaSb-finFET. It is observed from Fig. 5 that Ge-finFET exhibits lowest subthreshold swing value of 65.6 mV/dec at a drain voltage of 0.05 V. Reduced subthreshold swing in FinFET devices lies in its ability to lower power consumption, improve energy efficiency, enhance performance, increase design flexibility, and enhance the scaling potential of transistors.

The DIBL is defined as the difference in threshold voltage when the drain voltage is increased from 0.01 V to 0.05 V [20]. Drain induced barrier lowering (DIBL) value can be calculated using the relation reported in [18 - 19]:

$$DIBL(\frac{mV}{V}) = \frac{\Delta\ V_{TH}}{\Delta\ V_{DS}} \tag{4}$$

where V_{TH} is the threshold voltage and V_{DS} is the drain-source voltage.
The drain induced barrier lowering (DIBL) for Ge-finFET and GaSb-finFET have been plotted with respect to drain voltage as shown in Fig. 6. GaSb-finFET produces the lowest DIBL value of 5.35 mV/V at the drain voltage of 1 V as compared to the Ge-finFET. Reduced DIBL offer several advantages in finFET devices. Firstly, it enhances the threshold voltage roll-off property, ensuring more stable device performance. Secondly, it allows for the proper maintenance of the device's operating frequency, enabling efficient and reliable operation. Lastly, it effectively minimizes the short channel effect (SCE), mitigating any undesired effects that can occur in shorter channel

lengths. Together, these benefits contribute to the overall optimization and improved functionality of the device [22]

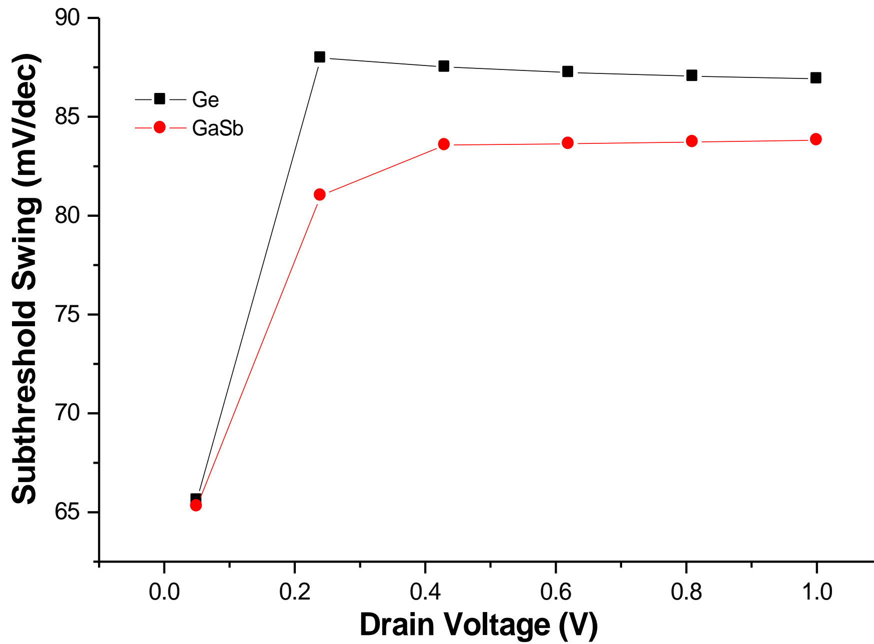

Fig. 5. Drain Voltage Vs Subthreshold Swing

3.5.Drain Voltage Variation with Drain Induced Barrier Lowering(DIBL)

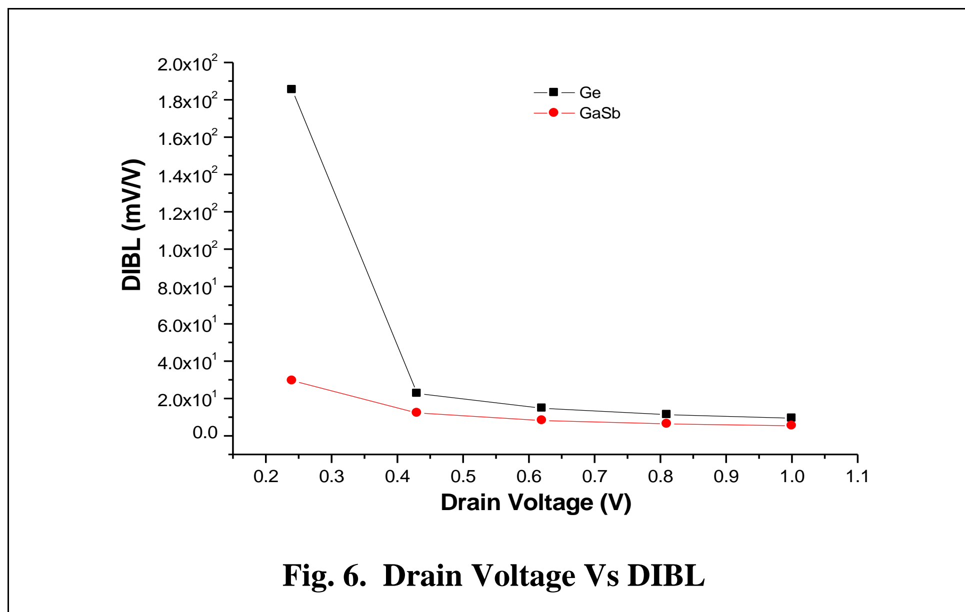

Fig. 6. Drain Voltage Vs DIBL

4. Conclusion

This paper has presented a comprehensive analysis of the performance of two potential channel materials, Germanium (Ge) and Gallium Antimonide (GaSb), in finFETs. Through simulations

conducted in the Padre Simulator environment, critical factors such as short channel effects, transconductance, and on-current were evaluated. The results of the study demonstrate that the GaSb-finFET outperformed the Ge-finFET in both transconductance and on-current, while also exhibiting reduced short channel effects; DIBL and threshold Voltage roll-off. However, Ge-finFET exhibits better SS characteristics. These findings are of great significance for applications that require rapid switching capabilities and have the potential to drive further research and development in the field of semiconductor technology. Overall, the study highlights the importance of channel material selection in the design and optimization of finFETs and underscores the potential benefits of exploring alternative materials for electronic device development. The reliability and robustness of Ge and GaSb FinFET devices, which are emerging materials for advanced transistor technologies, are important aspects to consider in order to ensure their successful integration in various electronic applications. Future research efforts can be directed towards conducting comprehensive analyses of the long-term stability, aging effects, thermal behavior, and variability of these devices, which will provide valuable insights into their performance under prolonged operational conditions.

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