Journal of Science and Technology Research

Journal homepage: www.nipesjournals.org.ng

Design of A High Efficiency Half-Bridge LLC Resonant Converter for Low Power Application

Bello N.[1*] and Edegbe E.[1]

[1]Department of Electrical and Electronic Engineering, Faculty of Engineering, University of Benin, PMB 1154, Benin City, Nigeria.

[*]Corresponding Author Email: nosabello@uniben.edu

Article Info

***Keywords*:**
LLC converter, low-power, efficiency, resonant capacitor.

Received 10 Sept. 2021
Revised 28 Sept. 2021
Accepted 30 Sept. 2021
Available online 10 June 2022

NIPES JOURNALS

https://doi.org/10.37933/nipes.e/4.2.2022.8

https://nipesjournals.org.ng

Abstract

The half-bridge (HB) LLC resonant converter is widely used in high and medium power applications, because of several advantages such as zero-voltage-switching (ZVS) capability over a wide input range and low component count. Most LLC resonant converters employ frequency modulation scheme to regulate the output power. However, in wide input voltage applications with widely varying hold-up time requirement, large switching losses are incurred during low power applications, which results in a low overall efficiency. A variable magnetizing inductance has been proposed for certain applications. However, this is not easy to implement as the relationship is not linear. This paper proposes a high efficiency, high power density half-bridge LLC resonant converter at low power application. High efficiency is reached at all power levels by introducing an operating mode: Low-power mode. Here, the output power is regulated by adjusting the voltage across the primary resonant capacitor. This provides for accurate mode control and linear power control. This method provides flexibility and ease of design for applications with largely varying power level requirement.

1. Introduction

High efficiency and power density have long been expected in server power supplies. Some organizations have developed strict guidelines for limiting high power usage of power supplies in order to meet the ever-present challenges. The Climate Savers Computing Initiative (CSCI), in particular, is establishing efficiency standards for computing and server systems [1]. The highest efficiency is expected under half load conditions, and a requirement for efficiency under 20% load conditions has been reinforced. In addition, a new performance guideline for 10% load conditions has been introduced. Since the server system runs at light-load conditions for several hours, this trend shows that light-load performance is becoming more significant [1]. The demand for high-quality, reliable, lightweight, and efficient power supplies is on the rise. LLC resonant converters have gained popularity in recent years due to their high efficiency at medium and high output loads. They have zero-voltage-switching (ZVS), smaller turn-off switching losses, soft commutation of the secondary rectifiers, a small-sized transformer, and low voltage strains on the primary switches, which are all desirable properties for high efficiency and high-frequency operation. However, the half-bridge (HB) LLC converter has a critical limitation of optimizing for efficiency in wide-input-voltage applications [2]-[3].

The main structure of the HB LLC resonant converter consists of an electromagnetic interference (EMI) filter, a boost converter with power factor correction, and an isolated dc-dc converter. Due to its high efficiency, high power density, low EMI, and wide input voltage range, the LLC resonant converter is a very convenient topology for DC-DC power conversion [4].

A resonant DC-to-DC converter produces sinusoidal currents with low switching losses. It allows operation at higher frequencies with excellent efficiency at high power levels. The pulse-frequency modulation (PFM) scheme is commonly employed in LLC converters to regulate the output power. While high efficiency is obtained at the resonant frequency due to low circulating current and soft-switching, the efficiency degrades when the switching frequency deviates from the resonant frequency which may result from wide variation in the input and output conditions [4].

A combination of different power regulation scheme has been proposed to boost the overall efficiency in ultra-low power application converters by [5]. They compared the schemes where both the pulse-frequency modulation (PFM) and pulse-width modulation (PWM) schemes are employed with a single control scheme model. This is frequently done to expand the load range that a converter can handle. The model can be used in a variety of different combinations. Efficiency in power converters is a very important consideration. It has an effect on the thermal and electrical losses in the device, as well as the amount of cooling needed. It also has an effect on the physical package size of the power supply and the whole device [6].

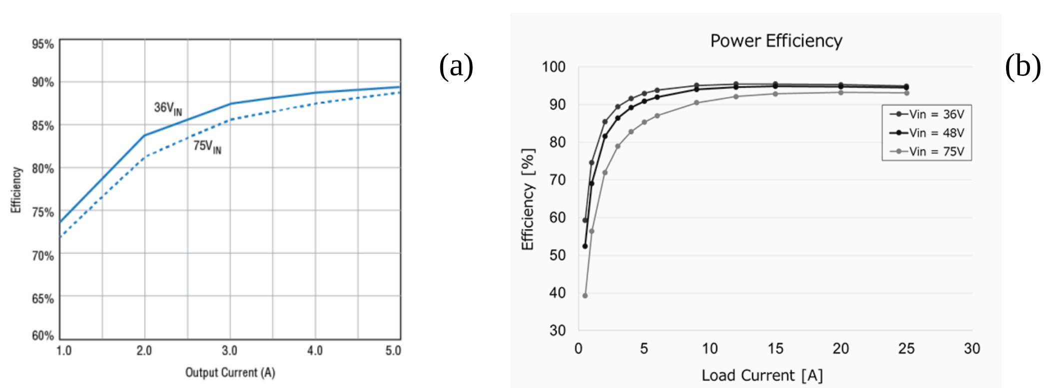


Figure 1. Typical efficiency curves of DC-DC converters [6]-[7]

The recurring drawback of most designs improving the efficiency of the LLC resonant converter is that, while high efficiency is achieved at high load over a wide voltage range, efficiency is poor at light load conditions. This paper proposes a HB LLC resonant converter with high efficiency even at low output load, standby, or no-load operation and this is achieved by employing a three-mode operation-mode transition is determined by the resonant capacitor voltage as a reflection of the transition in output load conditions or output power requirement.

2. Methodology

The output power of the converter is regulated by the voltage across the resonant capacitor (V_{Cr}). The output power and V_{Cr} have a linear relationship. The primary current (I_{Cr}) that drives the power conversion directly causes voltage variations on the resonant capacitor. The varying resonant capacitor voltage signal is harnessed to drive a mode transition in the power control scheme.

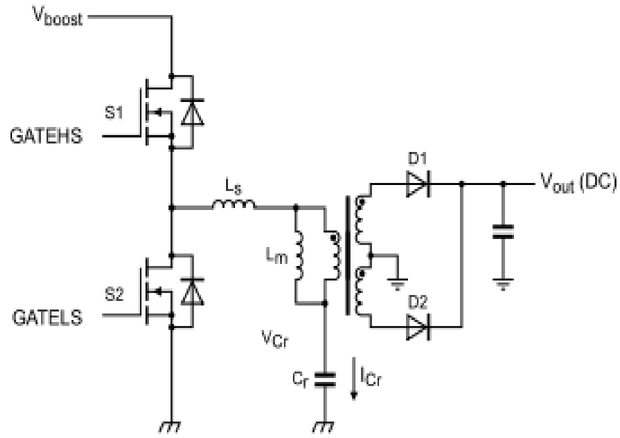


Figure 2. P_{out} and V_{Cr} have a linear relationship [2]

NXP semiconductors' TEA19161T half bridge LLC resonant controller is used to implement this power control process. The TEA19161T and TEA19162T work together to form a control combo-IC. A half-bridge controller for a resonant LLC tank and a PFC controller are included in the combo-IC to ensure high efficiency at all power levels. A high-performance resonant power supply has been constructed using the combination together with the TEA1995T dual LLC resonant synchronous rectifier (SR) controller.

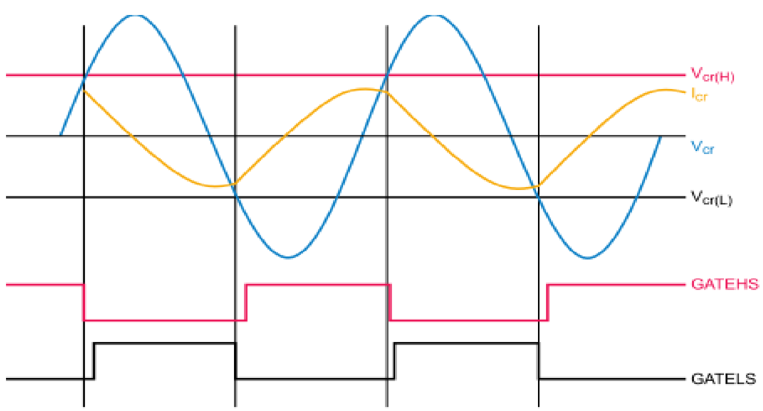


Figure 3. Gate drive control mechanism [2]

With a lower output voltage, the peak efficiency of an inductor-based DC-DC converter falls. The converter's switching and conduction losses stay constant for a given load current. At lower voltages, the output power level is reduced, resulting in a reduction in efficiency [5]. The power can be regulated by turning off the gate drive when the primary current reaches a certain level. The system feedback, in conjunction with the V_{Cr} signal, is used to control the gate driver for the power MOSFETs for higher or lower power.

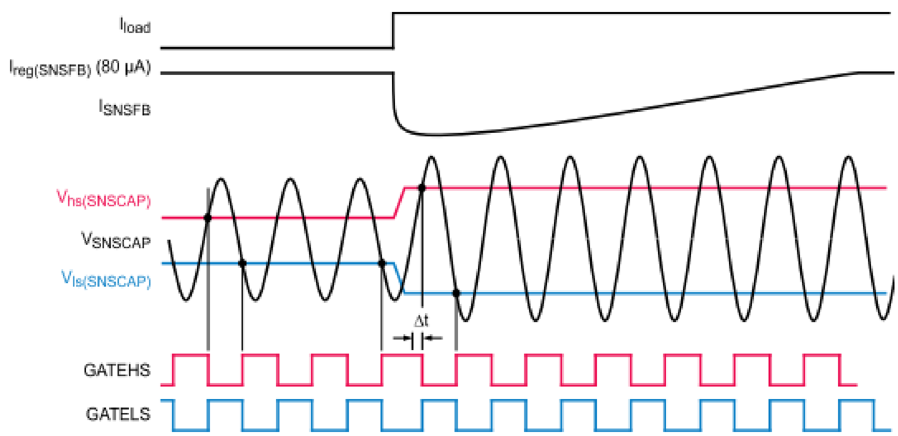


Figure 4. Load current change effect [2]

The voltage on the resonant capacitor is sensed by a resistive and capacitive divider. A resistive divider in parallel offers DC information. The signal's form is preserved with the capacitive divider.

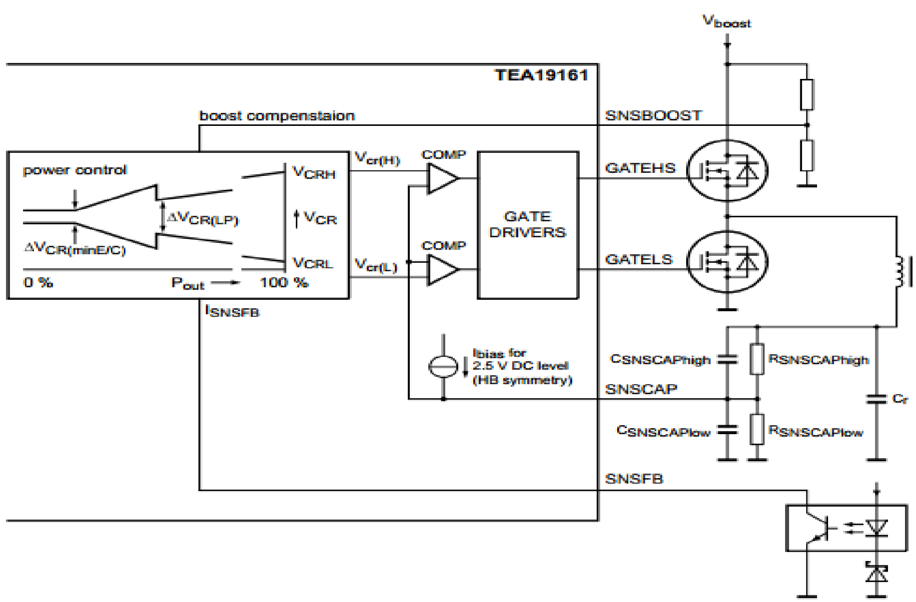


Figure 5. The gate driver circuit and external pre-sets [2]

The values of the divider are selected to scale the voltage range for the output power to a suitable range about a bias point - 3 V range in this case. This is because the SNSCAP pin is internally biased to 2.5 V, the minimum voltage on the pin is 1 V while the maximum voltage on the

SNSCAP pin is 4 V.

2.1. Low-Power Mode and Burst Mode Operation

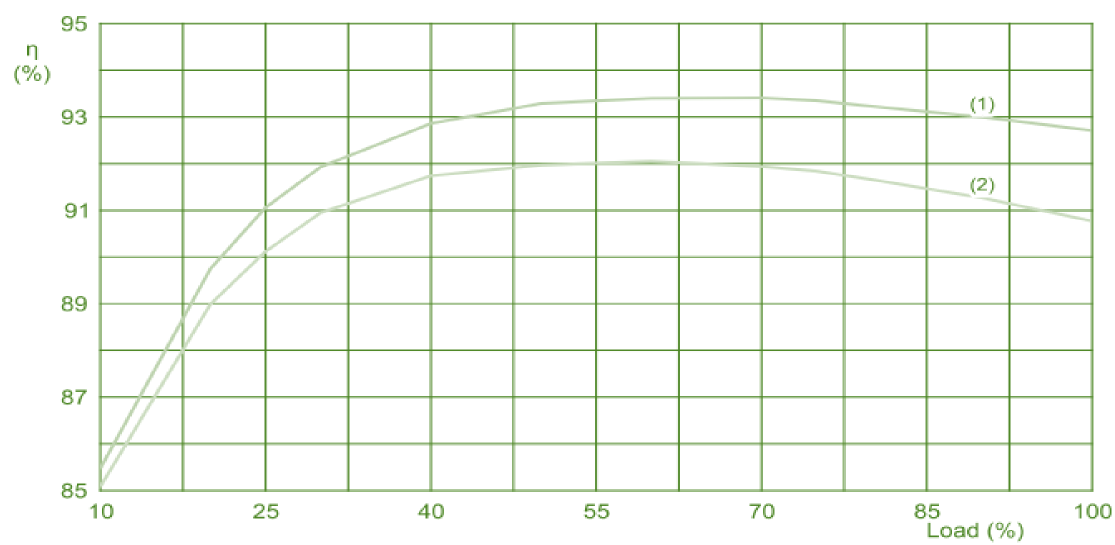
To reach a high efficiency at medium/low and standby output power, the low-power mode and burst mode are used. The behaviour of the half-bridge converter in low-power mode differs from the normal behaviour at maximum output power. As a result, the efficiency is near to the projected efficiency at higher load. The power level for leaving the high-power mode and entering the low-power mode can be adjusted. Here the power level is set at 53.4 W. Below 21.3 W, the power converter enters burst mode, which improves the overall efficiency at lower output loads.

3. Results and Discussion

To determine the efficiency, the input and output voltages and currents were measured.

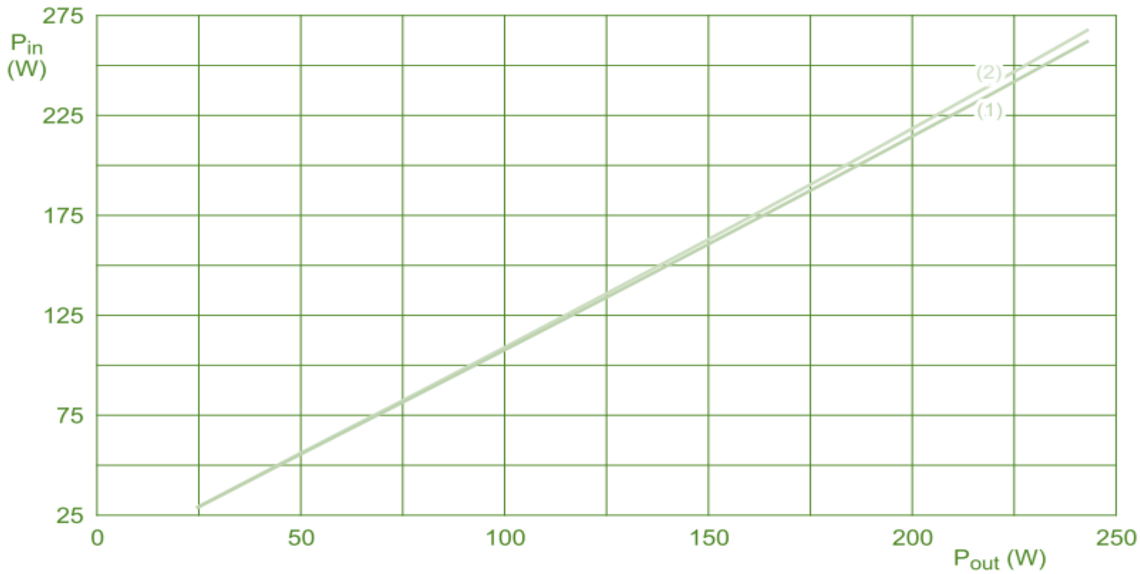
Table 1: Efficiency characteristics

Input Condition	Average	25% Load	50% Load	75% Load	100% Load
115 V/ 60 Hz	91.17	90.12	91.97	91.84	90.77
230 V/ 50 Hz	92.6	91.06	93.29	93.2	92.71



1. V_{mains} = 230 V (RMS)
2. V_{mains} = 115 V (RMS)

Figure 6. Efficiency curve



1. V_{mains} = 230 V (RMS)
2. V_{mains} = 115 V (RMS)

Figure 7. Power consumption

3.1. No-Load Power Consumption

Power consumption at no load was measured and record as in Table 2.

Table 2. Output voltage and power consumption at no load Condition

Input Condition	Output voltage	Power consumption
115 V/60 Hz	12.2 V	46 mW
230 V/50 Hz	12.2 V	51 mW

3.2. Standby Load Power Consumption

Power consumption at standby load was measured and record as in Table 3.

Table 3. Output voltage and power consumption at standby load Condition

Input Condition	Output Voltage	Power Consumption
115 V/60 Hz	12.2 V	356 mW
230 V/50 Hz	12.2 V	357 mW

Overall, from Figure 6, the efficiency of the proposed HB LLC resonant converter is improved over the load conditions until it peaks at 70% load beyond which it drops almost linearly. However, the efficiency of the 230V/50Hz input condition is higher than that of the 115V/60Hz input condition with an average value of 92.6% compared to 91.17% efficiency of the latter.

Correspondingly, the power consumption plot in Figure 7 shows that the 230V/50Hz input is better than the 115V/60Hz input. This is expected as the efficiency of the 230V/50Hz input condition is higher than that of the 115V/60Hz input. Overall, there is a linear relationship between the power input and the power output of the HB LLC power converter such that as the slope increases, the power output lags behind the input power much more. Therefore, as the slope increases the efficiency drops and so the 230V/50Hz input condition has a better power consumption as the input power increases.

In general, the efficiency of HB LLC circuits is high and a similar study done by [8] has shown an average efficiency of about 93% for all load conditions and an overall increase in efficiency as the load increases.

4. Conclusion

In this paper, a HB LLC resonant converter with high efficiency at all power level is proposed. It uses a control mechanism that modulates the gate drive of the primary switches using the output voltage feedback and the resonant capacitor voltage level. At a very moderate power density, low power and standby efficiency almost as high as that obtained in high power application was obtained. As a result, the suggested technique should be particularly appealing for high power density and high efficiency applications, such as server power supplies that require a high low-power efficiency specification.

Acknowledgement

The authors wish to acknowledge the effort of the staff of Electrical/Electronic Engineering, University of Benin, for the support, thereby making it easier to complete this journal.

Conflict of Interest

There is no conflict of interest associated with this work.

References

[1] Y. Jeong, G. W. Moon, and J. K. Kim, “Analysis on half-bridge LLC resonant converter by using variable inductance for high efficiency and power density server power supply,” Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC, pp. 170–177, 2017, doi: 10.1109/APEC.2017.7930689.

[2] NXP Semiconductors, “AN11801 TEA19161 and TEA19162 controller ICs,” 2019.

[3] C. E. Kim, J. Il Baek, and J. B. Lee, “High-Efficiency Single-Stage LLC Resonant Converter for Wide-Input-Voltage Range,” IEEE Trans. Power Electron., vol. 33, no. 9, pp. 7832–7840, 2018, doi: 10.1109/TPEL.2017.2772443.

[4] L. A. D. Ta, N. D. Dao, and D. C. Lee, “High-Efficiency Hybrid LLC Resonant Converter for On-Board Chargers of Plug-In Electric Vehicles,” IEEE Trans. Power Electron., vol. 35, no. 8, pp. 8324–8334, 2020, doi: 10.1109/TPEL.2020.2968084.

[5] A. Shrivastava and B. H. Calhoun, “A DC-DC converter efficiency model for system level analysis in ultra low power applications,” J. Low Power Electron. Appl., vol. 3, no. 3, pp. 215–232, 2013, doi: 10.3390/jlpea3030215.

[6] S. Davis, “Chapter 2: Power Supply Characteristics,” Power Management. https://www.powerelectronics.com/technologies/power-electronics-systems/article/21864107/power-management-chapter-2-power-supply-characteristics (accessed May 26, 2021).

[7] Toshiba Electronic Devices & Storage, “300W Isolated DC-DC Converter,” 2021. https://toshiba.semicon-storage.com/content/dam/toshiba-ss/shared/image/design-support/referencedesign/3-RD024-02.png (accessed May 26, 2021).

[8] Lee, J.B., Baek, J.I., Youn, H.S., Yeon, C.O., Lim, C.Y. and Moon, G.W., 2015, June. A high efficiency half-bridge LLC converter with simple hold-up compensation circuit. In 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia) (pp. 227-232). IEEE