NIPES

Journal of Science and Technology Research

Journal homepage: www.nipesjournals.org.ng

Investigation of the Thermal Effect in Nano Silicon on Insulator (SOI) MOSFET

S.M.Gana [a*], G.S.M.Galadanci [a], T. H. Darma [a], A. Tijjani [a]

[a] Physics Department, Bayero University Kano, P.M.B 3011, Kano

*Corresponding Author: smgana.phy@buk.edu.ng

Phone Number: +2348037504446

Article Info

***Keywords*:**
SOI-MOSFET, Average Electron Velocity, Electron velocity, Electron Density, Sub-Band Energy

Received 26 September 2021
Revised 26 October 2021
Accepted 23 November 2021
Available online 12 December 2021

https://doi.org/10.37933/nipes/3.4.2021.5

https://nipesjournals.org.ng

Abstract

This paper studied and investigates the thermal effect on the electronics and transport properties of Silicon on Insulator Metal Oxide Semiconductor Field Effect Transistor (SOI MOSFET). Numerical simulations of the electronics characteristics (Average electron velocity, electron density, sub-band energy) are analyzed and presented. The simulation is to investigate the variation and effect of temperature covering a range of low, average and high temperatures (50K, 250K, 350K, 450K, 650K and 850K) on the electronics properties of SOI MOSFET using the quasi-ballistic electron transport model. The results obtained showed that the average electron velocity of the first valley electron is at the peak value of $8.20 \times 10^5 m/s$ *at 50K and the 2D electron density is* $6.04 \times 10^{11} Cm^{-2}$ *at 850K with sub-band energy of* $-1.86 \times 10^{-1} eV$ *resulting in high on-state current (*I_{on}*). The second valley electron exhibit the same behaviour as the first valley electron with a 2D electron density of* $9.83 \times 10^{11} Cm^{-2}$ *at 850K. At average, low and high temperature the third valley electron from the source to the drain drift with an average electron velocity at the peak value of* $9.20 \times 10^5 m/s$ *at and the 2D electron density is* $6.03 \times 10^{11} Cm^{-2}$ *with sub-band energy of* $-1.21 \times 10^{-1} eV$ *resulting in high on-state current (*I_{on}*). This shows at a lower temperature the electron density is very low and almost constant through the channel region because of the high electron velocity. At an average temperature, the average electron velocity is relatively constant and the barrier potential is high as such the electron density is relatively constant with increase in the channel length which is more appropriate for designing other analogue or digital system using the SOI MOSFET. The average electron velocity at high is relatively constant as the channel length increases with increases in the gate voltage.*

1. Introduction

Silicon-on-insulator (SOI) technology has long been used in many special applications, and mainstream semiconductor products such as microprocessors, high performance integrated circuits, low-voltage, low power and high-speed digital systems [1]. The silicon-on-insulator (SOI) materials are now intensively studied because of their ability to overcome several inherent limitations of bulk silicon VLSI technology (lateral isolation, radiation tolerance, lower parasitic

capacitance and power, higher speed, reduced short-channel effects compared with the bulk device. Its architecture is more flexible as parameters such as thicknesses of film and buried oxide, substrate doping, and back gate bias can be used for optimization and scaling [1, 2]. The short channel effect (SCE) of SOI is minimized by burying oxide to reduce the electric field caused by Drain-Source ends such that the electric field line is not propagated through the channel but the oxide and hence have better control of the field over the channel [3].

The effect of temperature on SOI has been discussed in various literature. The effect of high-temperature and self-heating in fully depleted SOI MOSFET is studied by [4] and it was observed that decreasing the film thickness could reduce the threshold voltage sensitivity of the SOI MOSFET with temperature and that the drain current decreases with increasing temperature and self-heating effects reduced at a higher operating temperature. Temperature effects on Trigate SOI MOSFETs reported by [5] suggest that the mobility is limited for temperatures larger than 100 K, by surface roughness below that temperature and the device is fully depleted and does not suffer from premature corner inversion at temperatures above 150 K. Below 150 K the corners have a lower threshold voltage than the top and sidewall Si/SiO interfaces and the temperature at which the separation between corner and surface thresholds separate is a function of doping concentration. A study by [2] on temperature effects on Threshold voltage and mobility for partially depleted SOI MOSFET and reported that at low temperature the threshold voltage and mobility Improve for a particular gate length and long channels reach into full depletion-mode at a higher temperature as compared to short channels. In the previous researches conventional transport models (Drift-diffusion), can fail for ultra-short channel devices (Nano Devices) [6].

The objective of this research is to use the quasi-ballistic model to study the effect of temperature on silicon-on-insulator (SOI) MOSFET with physical gate length from 0nm to 50nm covering a temperature range of 50K, 250K, 350K, 450K, 650K and 850K. Study the electron behaviour within the temperature range to obtain the first, second and third valley average electron velocity, 2D electron density along the channel and the sub-band Energy along the channel using silicon (Si) as channel material.

2. Theoretical models

The unidirectional thermal velocity plays an important role in transport. Under equilibrium, the thermal average velocity of electrons with positive velocities is zero [7, 8]. Below the threshold, the Maxwell Boltzmann statistics as assumed and the thermal velocity (ν_T) is given by;

$$\nu_T = \sqrt{2k_B T/\pi m^*} \tag{1}$$

where the effective mass is m^*, the average carrier velocity at the beginning of the channel is the equilibrium, uni-directional thermal velocity [7, 9]. Assuming that only one sub-band is occupied the thermal injection velocity ($\widetilde{\nu_T}$) at the top of the barrier is given by;

$$\widetilde{\nu_T} = \nu_T \left(\frac{\mathcal{F}_{1/2}(\eta_{F1})}{\mathcal{F}_0(\eta_{F1})} \right) \tag{2}$$

The unidirectional thermal velocity in the non-degenerate limit is the same in 1D as in 2D and 3D and $\widetilde{\nu_T} \cong \nu_T$ and for degenerate conditions $\widetilde{\nu_T} > \nu_T$. Poisson's equation describes the spatial relationship between a certain electron density distribution and the corresponding electric field [10, 11].

$$\nabla^2 \emptyset = -\frac{1}{\epsilon}(p - n + N_D^+ - N_A^-) \quad (3)$$

where $\emptyset$ is the electric potential, p is the hole density, n is the electron density, N_D^+ is donor density and N_A^- is the acceptor density [12, 13]. When only the electrons are treated in the absence of holes Poisson's Equation is given by;

$$\nabla^2 \emptyset = -\frac{1}{\epsilon}(-n + N_D^+ - N_A^-) \quad (4)$$

The electron density at a certain energy level is defined as the product of the Local Density of State (LDOS) and Fermi distribution at that energy [14, 12].

$$n(E) = D(E)f(E) \quad (5)$$

where $n(E)$ is the electron density at energy E, $D(E)$ is the local density of state at energy E *and* $f(E)$ fermi distribution of the electron at energy E [12].

3. Methodology

In this paper, Nano-MOS a 2-D simulator for thin body devices is used. The channel material used is Si. The temperature is varied from a range of low temperature of 50K, and within the range of room temperature of 250K, 350K and 450K, then at a higher temperature of 650K and very high temperature for MOSFETS device at 850K. The result is obtained for a different channel length of 10nm, 20nm, 30nm, 40nm, and 50nm respectively. The source voltage is varied from 0.50V to 1.50V with a step size of 0.10V and the top and bottom gate contact work function was fixed at 4.188 eV with aluminium gate material, the top and bottom dielectric materials are SiO_2 [15]. The simulation for the variation in temperature is done using the following procedure;

1. The device is modelled by selecting device type (Double gate MOSFET)
2. Selecting transport model for the device geometry (ballistic transport using semiclassical Approach) and input bias parameters are inputted.
3. Devices description parameters are selected.
4. Simulation options are inputted (vertical and Horizontal Nodes spacing, convergence parameters, and Number of subbands).
5. The program is run to obtain results.

The transport model is solved self-consistently with Poisson's equation as described in Equation (3). The Poisson equation convergence parameter was $1.0E-06\ eV$ and the self-consistency convergence parameter was set at $0.001\ eV$. The body doping is intrinsic and the source and drain terminals are heavily n+ doped with arsenic at $1.0E12\ cm^{-3}$ to obtain the 2D electron density along the channel as given in Equation (4).

4. Results and Discussion

4.1 First Valley Average Electron Velocity

The average electron velocity along the channel for the first valley of electrons of Si channel material shows a rapid increase in the average electron velocity from $0.0nm$ and reach a peak value of $8.30 \times 10^5\ m/s$ at $51.0nm$ for 50K of temperature in Figure 1. This is because at low temperature the barrier potential is very high through the channel region near the source terminal, thus the electrons need high potential energy to cross over to the source terminal resulting in high velocity of the electron, the velocity becomes relatively constant with the smallest decrement around 48.0 to $51.0nm$ and becomes constant above $51.5nm$. At $250K, 350K\ and\ 450K$ the

average electron velocity is relatively constant as the channel length increases because at temperature range close to or at room temperature the barrier potential is loose which result in an averagely high on-state current (I_{on}) controlled by how rapidly the electrons are transported from the drain high electric field region to the source low electric field region.

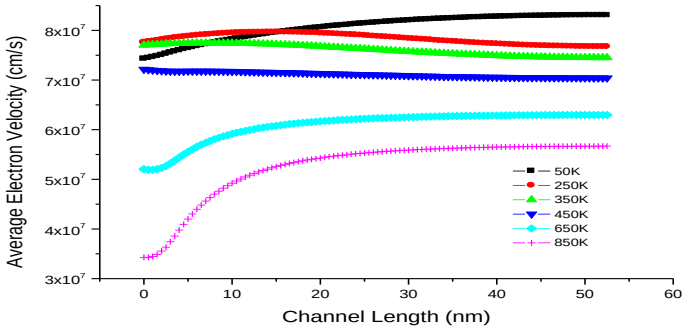

Figure 1: First Valley Average Electron Velocity

At high temperature $650K\ and\ 850K$ it is found out that the average electron velocity is at the lowest value and increases as the channel length increases before it becomes almost constant with the smallest decrement. This is because with the increase in channel length the barrier potential is low at high temperature it is easily suppressed for electrons to cross the channel region from the drain to the source. This is also reported by Ooi and King in 2013 that at low temperature the average velocity is at maximum peak value than at high temperature [16].

4.2 Second Valley Average Electron Velocity

In the second valley of electrons plot as shown in Figure 2 the average electron velocities in the second valley exhibit the same characteristics as the first valley of the electron at a temperature of 50K, 250K and 350K. Because in the second valley the electron is closer to the conduction band in the sub-band so are rapidly transported from the drain high electric field region to the source low electric field region. The average electron velocity at $450K, 650K\ and\ 850K$ exhibit the same behaviour as the first valley temperature of $650K\ and\ 850K$ as the channel length increases.

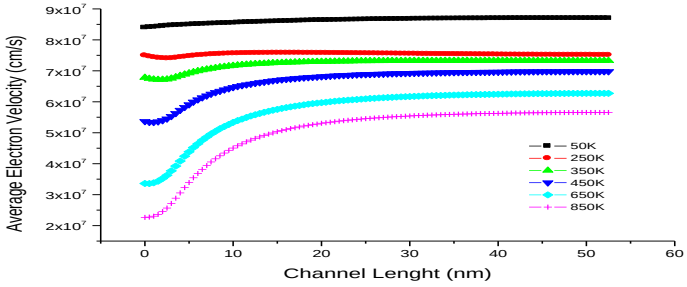

Figure 2: Second Valley Average Electron Velocity

4.3 Third Valley Average Electron Velocity

The average electron velocity at 50K as shown in Figure 3 is relatively constant with an average velocity of $9.20 \times 10^5\ m/s$ as the channel length increases for the third valley electron under high and low drain bias.

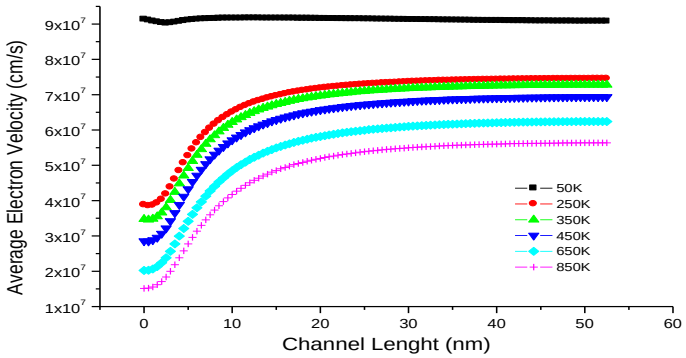

Figure 3: Third Valley Average Electron Velocity

At temperatures at 250K, 350K, 450K, 650K and 850K there are more free electrons at the third valley of electrons because, at the third valley of electrons, the electrons are much closer to the conduction band. As the gate voltage increases above $V_{GS} = 0.5V$ the average electron velocity increases before it becomes relatively constant with the smallest decrement above $10.5\,nm$ because the higher electron mobility at the channel region from the source high electric field region to the drain low electric field which result in an averagely high on-state current (I_{on}). This is in agreement with research by Jean-Pierre et al. in that the mobility of electrons is limited for temperatures larger than 100 K, while it is limited by surface roughness below that temperature [5].

4.4 First Valley 2D Electron Densities along the Channel

The electron density at high temperatures of 850K and 650K is at a peak value of $6.04 \times 10^{11} Cm^{-2}$ and $3.89 \times 10^{11} Cm^{-2}$ respectively from 0.0nm and decrease rapidly with an increase in the channel length in the first valley of an electron as shown in Figure 4. This is because at the lowest length region at high temperature the electrons are concentrated to overcome the barrier potential resulting in high electron density drifting from the drain to the source through the channel region before it becomes relatively constant At high temperature, the density of electrons is very high as such the electrons are concentrated at the lowest channel region ($0.0nm$) with a peak value of $3.383 \times 10^{12} cm^{-2}$ to overcome the barrier potential, but the barrier potential is very low at high temperate so even with gate voltage $V_{GS} = 0.5v$ large number of electrons easily overcome the barrier potential and drift from the drain to source through the channel region. At 50K, 250K, 350K and 450K the barrier potential is high at low and average temperatures as such the electron density is relatively constant with an increase in the channel length. This is because the average electron velocity as shown in Figure 1 is relatively constant as the channel length increases with increases in the gate voltage resulting increase in the potential electron profile which limit the number of electrons entering the channel region.

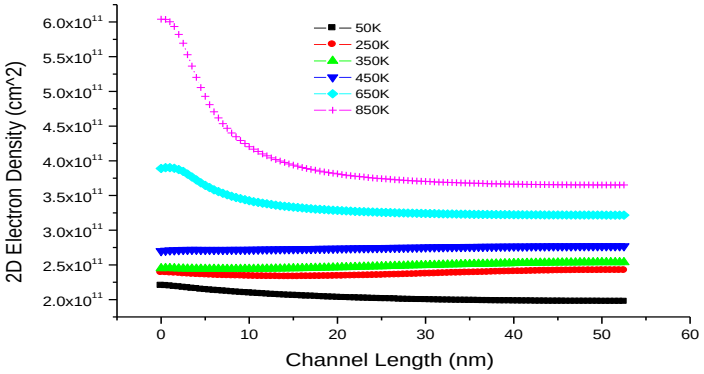

Figure 4: First Valley 2D Electron Velocity

4.5 Second Valley 2D Electron Densities along the Channel

The 2D electron density at 850K and 650K in Figure 5 shows that the second valley of electron exhibit the same behaviour as the first valley of an electron in figure 4 except that electrons are more concentrated at 0.0nm in the second valley of an electron with peak values of $9.83\times 10^{11}Cm^{-2}$ and $6.59\times 10^{11}Cm^{-2}$ respectively and decrease as the channel length increase. This is because in the second valley more free electrons are closer to the conduction band in the sub-band than in the first valley at high temperature. At 450K the 2D electron density is at the peak value of $4.07\times 10^{11}Cm^{-2}$ from 0.0nm to 3.5nm before it becomes almost constant above 14.5nm. At 50K, 250K and 350K the electron density is relatively constant with an increase in the channel length as can be seen from their average electron velocities in Figure 2 with average 2D electron densities of $3.89\times 10^{11}Cm^{-2}, 2.84\times 10^{11}Cm^{-2}$ and $3.00\times 10^{11}Cm^{-2}$ respectively.

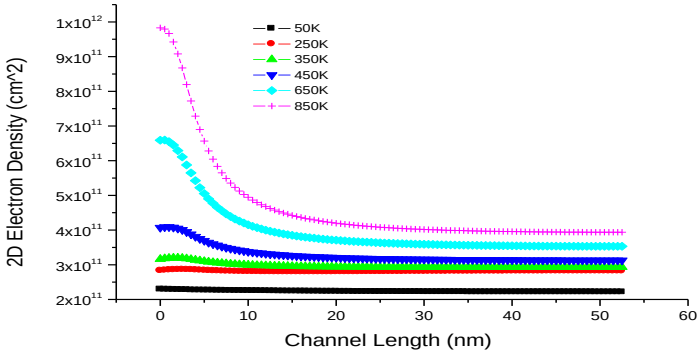

Figure 5: Second Valley 2D Electron Velocity

4.6 Third Valley 2D Electron Densities along the Channel

In the third valley in Figure 6 the 2D electron density at 850K, 650K, 450K, 350K and 250K are more concentrated at 0.0nm with peak values of $1.56\times 10^{12}Cm^{-2}$, $1.17\times 10^{12}Cm^{-2}$, $8.32\times 10^{12}Cm^{-2}$, $6.78\times 10^{11}Cm^{-2}$ and $6.03\times 10^{11}Cm^{-2}$respectively and decrease as the channel length increase. This is because at the third valley the electrons are much closer to the

conduction band as such more concentrated at the channel region with increases in temperature and the electron density is at peak at lowest resulting in a large number of electrons drifting from the drain to the source through the channel region by the suppression in the barrier potential.

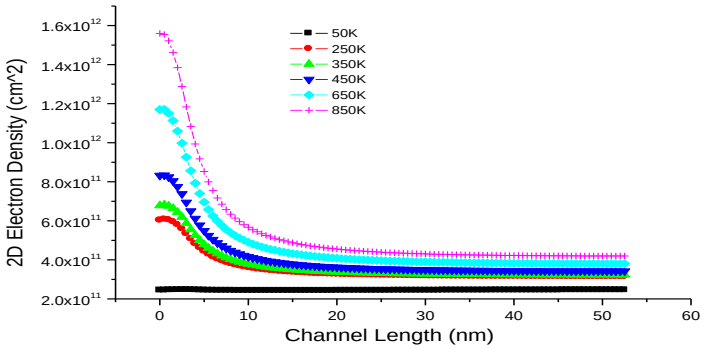

Figure 6: Third Valley 2D Electron Velocity

This is also reported in a research that at high temperature, the density of electrons is very high as such the electrons are concentrated at the lowest channel region to overcome the barrier potential, but the barrier potential is very low at high temperate so a large number of electrons easily overcome the barrier potential and drift from the drain to source through the channel region [15]. At a lower temperature of 50K the electron density is very low and almost constant through the channel region because of the high electron velocity as shown in Figure 3.

4.7 First Valley Sub-Band Energy along the Channel

The sub-band energy at low temperature $(50K)$ in the first valley of an electron in Figure 7 is average $-4.95 \times 10^{-1} eV$ because the potential barrier is very high and the average electron velocity is low as seen in Figure 1.

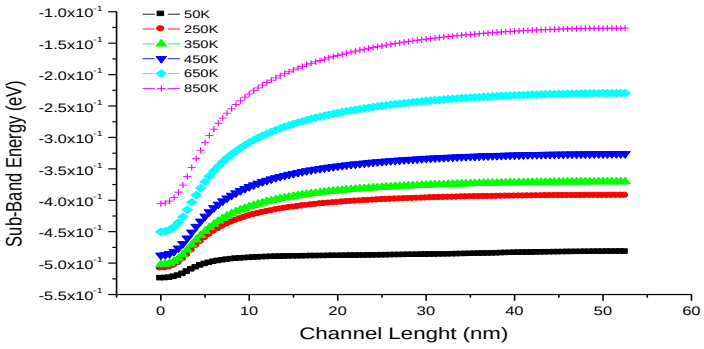

Figure 7: First Valley Sub-band Energy along the channel

The energy along the channel is also low with high electron density as described in Figure 4. As the temperatures increase from 250K, 350K, 450K, 650K to 850K the sub-band energy increases with an increase in the channel length, with sub-band energy of $-4.16 \times 10^{-1} eV, -3.98 \times$

$10^{-1}eV, -3.60 \times 10^{-1}eV, -2.76 \times 10^{-1}eV$ and $-1.86 \times 10^{-1}eV$ respectively. This is because as the temperature increases the drain bias is high by a significant increase in the gate voltage from $V_{GS} = 0.5v$ thereby lowering the energy and the high gate voltage lowers the potential energy barrier which allows electrons to flow from the source to the drain. It is also reported by Rahman et al. that the device exhibit a strong drain electron injection and the MOSFET is under the on-state condition because a high drain bias lowers the energy in the drain and a high gate voltage lower the potential energy barrier, which allowed electrons to flow from source to drain [17].

4.8 Second and Third Valley Sub-Band Energy along the Channel The behaviour of electrons in the second valley of an electron is similar to the first valley of electron and the sub-band energy exhibit the same characteristics as the sub-band energy in the second and third valley of electrons as can be seen in Figure 7 and Figure 8 respectively.

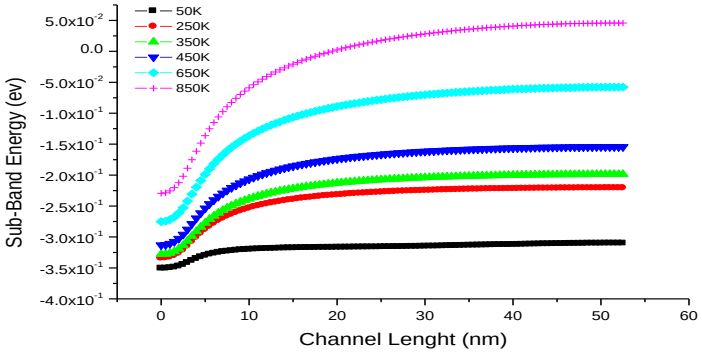

Figure 7: Second Valley Sub-band Energy along the channel

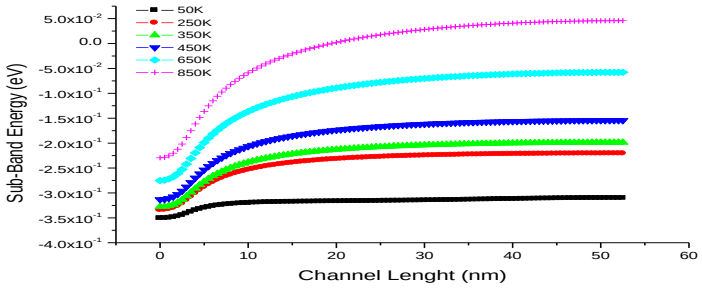

Figure 8: Third Valley Sub-band Energy along the channel

The electrons in the second and third valley of the electron are much closer to the conduction band as such the sub-band energy is a little higher than the first valley of an electron with an average sub-band energy of $-3.21 \times 10^{-1}eV, -2.43 \times 10^{-1}eV, -2.24 \times 10^{-1}eV, -1.86 \times 10^{-1}eV, -1.03 \times 10^{-1}eV$ and $-1.21 \times 10^{-1}eV$ for 50K, 250K, 350K, 450K, 650K to 850K respectively.

5. Conclusion

Numerical device simulations using Nano-MOS Version 4.0.4 have been performed to investigate the electron characteristics of SOI MOSFETs at 50K, 250K, 350K, 450K, 650K and 850K in this

paper. Based on the quasi-ballistic transport electron model the results obtained showed that at low temperature (50K) the electron density is very low and almost constant through the channel region with an average electron at the peak value of $8.20 \times 10^5 m/s$ in the first valley of the electron. At 250K, 350K, 450K the average electron velocity is relatively constant as the channel length increases because at temperature range close to or at room temperature the barrier potential is loose which result in an averagely high on-state current (I_{on}). At high temperatures, 650k and 850K the barrier potential is loose resulting in more free electrons at the third valley of electrons and the average electron velocity increases before it becomes relatively constant because of the higher electron mobility at the channel region from the source high electric field region to the drain low electric field which results in an averagely high on-state current (I_{on}).

Reference

[1] J. P. Collinge, "The New Generation of SOI MOSFETs," Romanian Journal of Information Science and Technology, vol. 11, no. 1, pp. 3-15, 2008.

[2] N. Goel and A. Tripathi, "Temperature effects on Threshold Voltage and Mobility for Partially Depleted SOI MOSFET," International Journal of Computer Applications, vol. 42, no. 21, pp. 56-58, 2012.

[3] M. Asmaa, "Analysis of temperature and high-frequency effects in Double-Gate MOSFETs," University: Rovira I Virgili, Tarragona Spain, 2013.

[4] A. K. Goel and T. H. Tan, "High-temperature and self-heating effects in fully depleted SOI MOSFETs," Microelectronics Journal (Elsevier), vol. 37, p. 963–975, 2006.

[5] C. Jean-Pierre, L. Floyd, A. J. Quinn, G. Redmond, J. C. Alderman, W. Xiong, C. Cleavelin, T. Schulz, K. Schriefer and G. Knoblinger, "Temperature Effects on Trigate SOI MOSFETs," IEEE ELECTRON DEVICE LETTERS, vol. 27, no. 3, pp. 172-174, 2008.

[6] A. Rahman and M. Lundstrom, A Compact Scattering Model for the Nanoscale Double-Gate MOSFET., School of Electrical and Computer Engineering Purdue University, West Lafayette, In 47907-1285., 2001.

[7] M. Lundstrom and Z. Ren, "Essential Physics of Carrier Transport in Nanoscale MOSFETs," IEEE Transaction Electron Devices, vol. 49, no. 1, pp. 133-141, 2002.

[8] C. Y. Ooi and S. K. Lim, "Study of Timing Characteristics of NOT Gate Transistor Level Circuit Implemented Using Nano-MOSFET by Analyzing Sub-Band Potential Energy Profile and Current-Voltage Characteristic of Quasi-Ballistic Transport," World Journal of Nano Science and Engineering, 6, pp. 177-188, 2016.

[9] O. C. Yee and S. K. Lim, "Simulation Study On The Electrical Performance Of Equilibrium Thin-Body Double-Gate Nano-Mosfet," Jurnal Teknologi, vol. 76, no. 1, p. 87–95, 2015.

[10] T. Hatakeyama and K. Fushinobu, "Electro-Thermal Behavior of a Sub-MicrometerBulk CMOS Device: Modeling of Heat Generation and Prediction of Temperatures," Internation Journal of Heat Transfer Engineering, vol. 29, no. 2, p. 120–133, 2008.

[11] A. A. Ziabari, M. Charmi and H. R. Mashayekhi, "The Impact of body doping concentration in the performance of Nano MOSFET: A Quantum Simulation," Chinese Journal of Physics, vol. 51, no. 4, pp. 844-853, 2013.

[12] Wang, "NanoMOS 4.0: A Tool To Explore Ultimate Si Transistors and Beyond," Purdue University, West Lafayette, Indiana, 2010.

[13] A. A. Ahmadain, K. P. Roenker and K. A. Tomko, "A Study of the Performance of Ballistic Nanoscale MOSFETS Using Classical and Quantum Ballistic Transport Models," Sixth IEEE Conference on Nanotechnology, Cincinnati, OH, USA, vol. 3, no. 6, pp. 16-19, 2006.

[14] Z. Ren, S. Goasguen, A. Matsudaira, S. S. Ahmed, K. Cantley, Y. Liu, Y. Gao, X. Wang and M. Lundstrom, "NanoMOS," 22 March 2006. [Online]. Available: https://nanohub.org/resources/nanomos.

[15] S. M. Gana, G. S. M. Galadanci, T. H. Darma and A. Tijjani, "Effect of Temperature on The Quasi Ballistic Transport of A Double Gate Nano-Mosfet," NIPES Journal of Science and Technology Research, vol. 3, no. 2, pp. 1-10, 2021.

[16] C. Y. Ooi and S. K. King, "Temperature Variation Effects In Nano-Mosfets Based on Simulation Study," International Journal of Education and Research, vol. 1, no. 2, pp. 1-17, 2013.

[17] A. Rahman, J. Guo, S. Datta and M. S. Lundstrom, "Theory of Ballistic Nanotransistors," IEEE Transactions on Electron Devices, vol. 50, no. 9, pp. 1853-1864, 2003.