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Investigation of Single-Phase, Single Voltage Source Multilevel Inverter with Voltage Boosting Gain Based on Different Sinusoidal Pulse Width Modulation Approach

G. C. Diyoke[a]*, O. Oputa[a], I. K. Onwuka[a], P. I. Obi[a]

[a]Department of Electrical and Electronic Engineering, Michael Okpara University of Agriculture, Umudike, P. M. B. 7267 Umuahia, Abia State, Nigeria. *Corresponding Author: geraldiyoke@mouau.edu.ng

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Abstract

This paper investigated a single-phase, single voltage source multilevel inverter with voltage boosting gain based on different sinusoidal pulse width modulation approach. This article is meant for selection of appropriate modulation technique for proposed multilevel inverter topology. The proposed approach is formed by combination of MOSFET power switches, dc voltage doubler circuit, power cables, pulse-width generator circuits and resistive-inductive load. The system is capable of producing an output voltage of three-level and five-level depending on the amplitude of the reference signal. Among other pulse-width modulation techniques investigated, the two carrier signals with high frequency and one rectified reference signal with low frequency is adopted for the work. This article is used to verify the output current and voltage amplitude, total harmonic distortions based on different modulation schemes. The overall system is modeled and simulated in MATLAB/SIMULINK environment. The outcomes of the investigations are that: (i) rectified reference multiple carrier (RRMC) pulse width modulation scheme resulted in 58.24 % Voltage total harmonic distortion (THD), and 14.58 % Current THD for three level operation; and 30.39 % Voltage THD and 7.76 % Current THD for five-level operation, with an output average voltages of 94.27 V and 189 V for three and five levels respectively; (ii) single-reference multiple carrier pulse width modulation scheme resulted in 58.29 % Voltage THD and 14.58 % Current THD for three level operation and 30.44 % Voltage THD and 7.75 % Current THD for five level operation; with an output average voltages of 93.27 V and 188.5 V for three and five levels respectively. Performance assessment of the adopted method is validated by comparing the simulation and experimental results.

1. Introduction

Recently, multilevel inverter configurations in industry and in electronic power conversion for high voltage applications [1]. This links industrial drive, high voltage dc transmission (HVDC), electric vehicle (EV), etc. Multilevel inverters play a vital role in mix-energy systems such as integrations of different sources of dc voltage sources, power factor corrections, etc. Due to reduced voltage stress on the power semiconductors devices for high voltage generation, reduced total harmonic distortions, the small size of the filter, reduced electromagnetic interference (EMI), improved efficiency, fault

tolerance and many more multilevel inverters play an important role in medium and high voltage applications [2]-[6]. Multilevel inverters (MLIs) have been an emerging power electronics technology with promising developments and growing importance for dc-ac electrical energy conversion system [7]-[8]. They are exceptionally popular for high/medium voltage applications and thus envisaged to continue garner continuous attention in the near future. Tremendous research works are ongoing for establishing new MLI topologies for various applications [9]-[10]. Awareness of the inherent potentials of MLIs and their positive impacts on series of industrial applications have led to the proliferation of multilevel inverter power circuit configurations, as reported in the literature, [11]-[13]. Critical assessment of these newly evolved MLI topologies shows that they are actually either a hybrid or an off-shoot of one of the conventional MLI configurations: cascaded H-bridge (CHB), diode-clamped and capacitor-clamped (flying capacitor) multilevel inverters [14]-[17]. Looking at the different types of multilevel inverters, they are characterized by high number of power switches which are associated with high power losses [18]-[22]. They are also accompanied by complex modulation schemes with high number of carrier signals. In quest to remove or reduce these number of power switches and at the same time boost the output voltage, switched- capacitor based multilevel inverter is introduced.

To overcome these issues, researchers have proposed a self-balanced switched-capacitor multilevel inverter (SCMLI), which can synthesize the desired voltage levels at the output using fewer components and reduced control complexity [23]-[28]. Voltage boosting is essential for the topologies to be used in the integration with renewable energy resources especially solar photovoltaic system due to its low voltage generation. In the case of lower solar photovoltaic (PV) voltages, a high gain DC–DC converter along with multilevel inverter can be used to boost the PV voltage for obtaining desired output voltage for grid integration [29]-[31]. Switched capacitor (SC) based multilevel inverter topologies with boosting feature gives a suitable approach for the low input voltage systems. In SCMLI, the switched capacitors are charged and discharged in parallel and series configurations with dc input supply voltage, respectively. However, authors in [32] reported that conventional MLIs require more components and more complex control circuitry due to voltage balancing issues with an increased number of levels at the output voltage [33]-[38]. Furthermore, SC-based topologies with self-voltage balancing of the capacitors without any auxiliary methods reduce the control complexity of the system have been reported by [39]-[40]. A switched-capacitor based on H- bridge has been proposed to generate a dual output voltage one at a time. The circuit is capable of generating ac output that is equivalent of supply dc and twice supply dc voltage values respectively. This function is obtained from the pulse-width modulation scheme adopted. The combination of the power circuit and control scheme makes the system to be fault tolerance.

Different sinusoidal pulse width modulation (SPWM) techniques [41]-[49] were looked at among them include: firstly, rectified reference multiple carrier (RRMC) SPWM which was discussed in details in this work. Secondly, phase disposition PD-SPWM, here all the carrier signals are in phase and level shifted. For five-level application, it contains four carrier signals and one modulating signal. Thirdly, alternate phase opposition disposition (APOD) SPWM modulation scheme is very similar to PD SPWM; however, the carrier signals are phase displaced from one another by 180o degrees alternatively. This method contains four carrier and one modulating signals. Fourthly, phase opposition disposition (POD) SPWM, here, the carrier signals above the reference or zero line are in the same phase and the carrier signals below the zero line are in the same phase, but the carriers below and above the zero line are out of phase by 180o Fifthly, multi-reference single carrier (MRSC)

SPWM, this modulation scheme contains two reference signals and one carrier signal. The carrier signal is placed above zero or reference line and the rectified reference signal is placed above zero line. Therefore, the reference signal is level shifted by the negative value of the carrier signal. Lastly, single reference multiple carrier (SRMC) SPWM modulation scheme, the two carrier signals are in phase, level shifted and placed above reference line. The reference signal denoted takes the shape of half sine wave in the first half cycle and inverted half sine wave in the remaining half cycle. Comparisons of the reference and carrier signals generate the required firing pulses for the different inverter power switches.

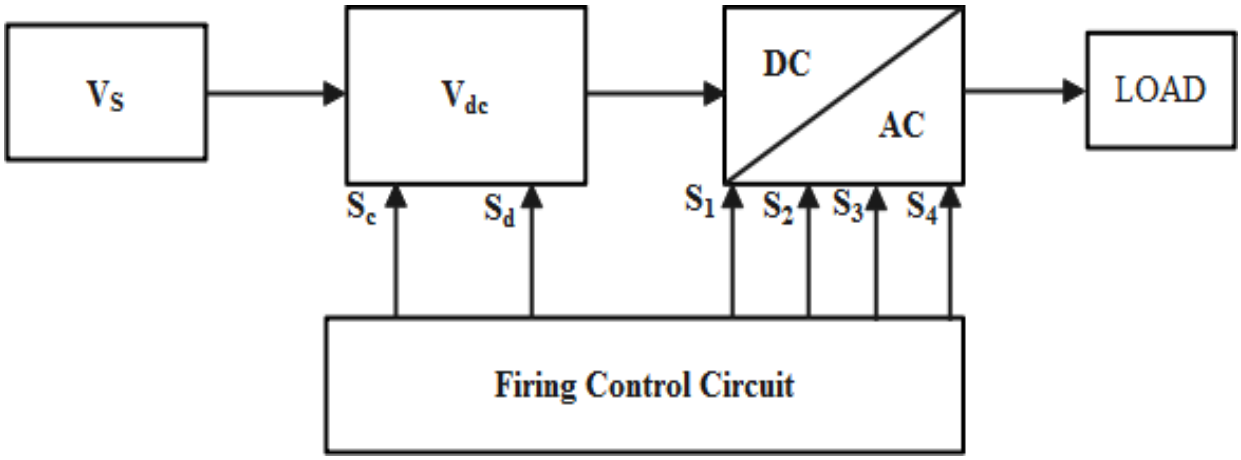

Fig. 1: Block diagram for the proposed multilevel inverter system

To fill some of research gaps and obtain dual ac output voltage, the paper is organized as follows: introduction and block diagram of the proposed topology. Section two (2) proposes the materials and method adopted to realize the aim; such as the operational principle and modulation strategy. Thereafter, the simulation results and comparative information between the different modulation techniques are depicted in Section three (3), Section four (4) shows the research experimental results which validate the simulation results and finally, summary and conclusions were made in section five (5).

2. Methodology

2.1 Circuit Model Formulation

Shown in Fig. 2 is the power circuit of the proposed multilevel inverter configuration. It comprises of an H-bridge, a capacitor bank, simplified charge-discharge circuit, a dc source, and resistive-inductive load. Two active switches and a diode are the components of the charge-discharge unit. One of the switches contains no free-wheeling diode. The function of this switch is to maintain a unidirectional discharge of the capacitor bank. The two switches are connected in a half-bridge fashion whose node links the capacitor bank.

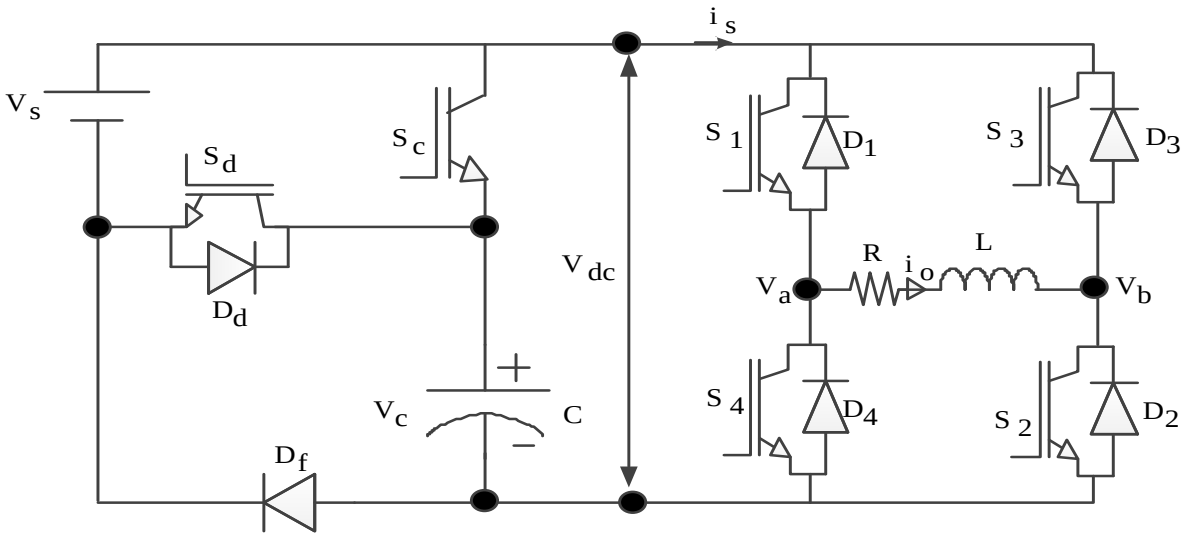

Fig. 2: Power circuit diagram for the proposed multilevel inverter system

The diode interconnects the negative polarity of the capacitor bank and of the H-bridge inverter to the negative terminal of the input voltage source.

2.2 Operational principle

With the arrangements of the circuit components as depicted in Fig. 2, the H-bridge and the charge-discharge circuit in the inverter under proper control can generate five level output voltage as: 0, Vs, 2Vs, -2Vs, -Vs. Also, under good adjustment of the amplitude of the reference signal, three level output voltage as: 0, Vs and –Vs can be generated. The operational modes of the circuit topology, switching states and synthesized output voltages are detailed in [50].

2.3 Modulation scheme

In this subsection, rectified reference multiple carrier (RRMC) sinusoidal pulse width modulation (SPWM) schemes are displayed. In this SPWM modulation scheme, it contains one rectified reference and two carrier signals. The two carrier signals are in phase, level shifted and placed above reference line as depicted in Fig. 3 and are represented as Vcr1 and Vcr2. The reference signal is a rectified sine wave placed above zero line.

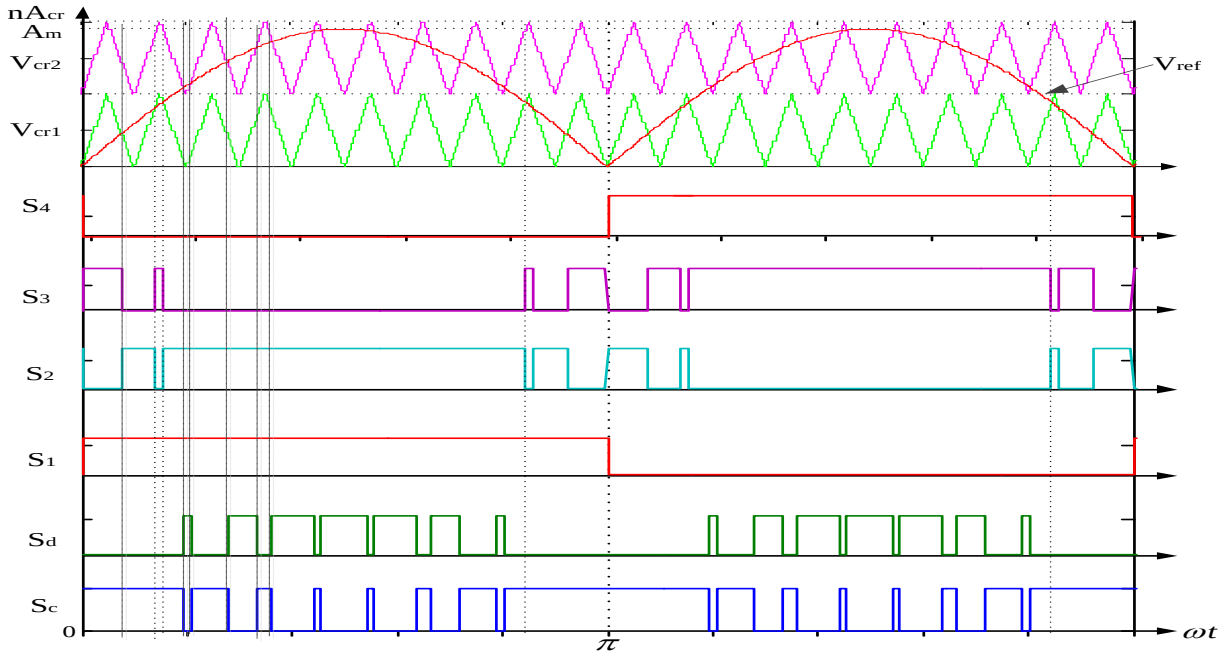

Fig. 3: RRMC SPWM modulation technique for single phase five level inverter.

Comparisons of these two carrier signals with the corresponding modulating signal generates the control signals, which have to be assigned to a particular inverter power switch gates. The logic circuit diagram is as shown in Fig. 4. It contains triangular and sine wave generators, two level shifters, absolute value function, three comparators, four NOT gates, two AND gates and one OR gate.

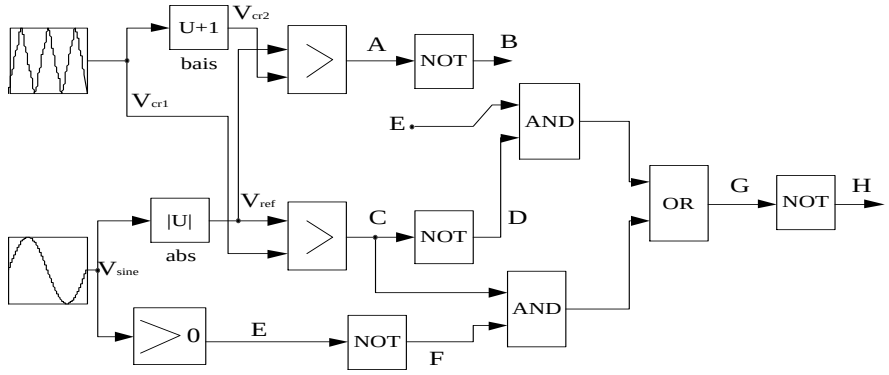

Fig. 4: Logic circuit

The mathematical logic expressions are shown in equations (1 - 8).

$$A = V_{ref} > V_{cr2} = S_d \quad (1)$$

$$B = \overline{A} = S_c \quad (2)$$

$$C = V_{ref} > V_{cr1} \quad (3)$$

$$D = \overline{C} \quad (4)$$

$$E = V_{\sin e} > 0 = S_1 \quad (5)$$

$$F = \overline{E} = S_4 \quad (6)$$

$$G = D \bullet E + C \bullet F = S_3 \quad (7)$$

$$H = \overline{G} = S_2 \quad (8)$$

3. Results and Discussion

3.1 Simulation results

The simulation based on MATLAB/SIMULINK is performed for the proposed topology. The simulation of the circuit configuration is carried out under various SPWM schemes mentioned in section 2. The simulation results depicted in this section is based on RRMC SPWM technique. The simulation of this technique is carried out under (a) five –level output voltage waveform, and (b) three-level output voltage waveform. The power circuit in Fig. 2 was used to demonstrate the features of the proposed five-level single phase inverter topology; wherein the switching scheme depicted in Fig. 3 was utilized. The simulations were carried out with arbitrary R-L load; R and L are 25 Ω and 4 mH respectively. The carrier/switching frequency is 3 kHz. The dc input voltage, Vs is 100 V and the capacitor, C, has a capacitance value of 4700 µF.

3.1.1 Simulation Results based on Five-level Output Voltage

Fig. 10 and Fig. 11 show the simulated five-level voltage and current waveforms for modulation index of 0.95. The spectral analyze result of this synthesized inverter output waveform in Fig. 10 (e) is displayed in Fig. 12. Therein, THD value of 30.39% is achieved in five-level output voltage waveform.

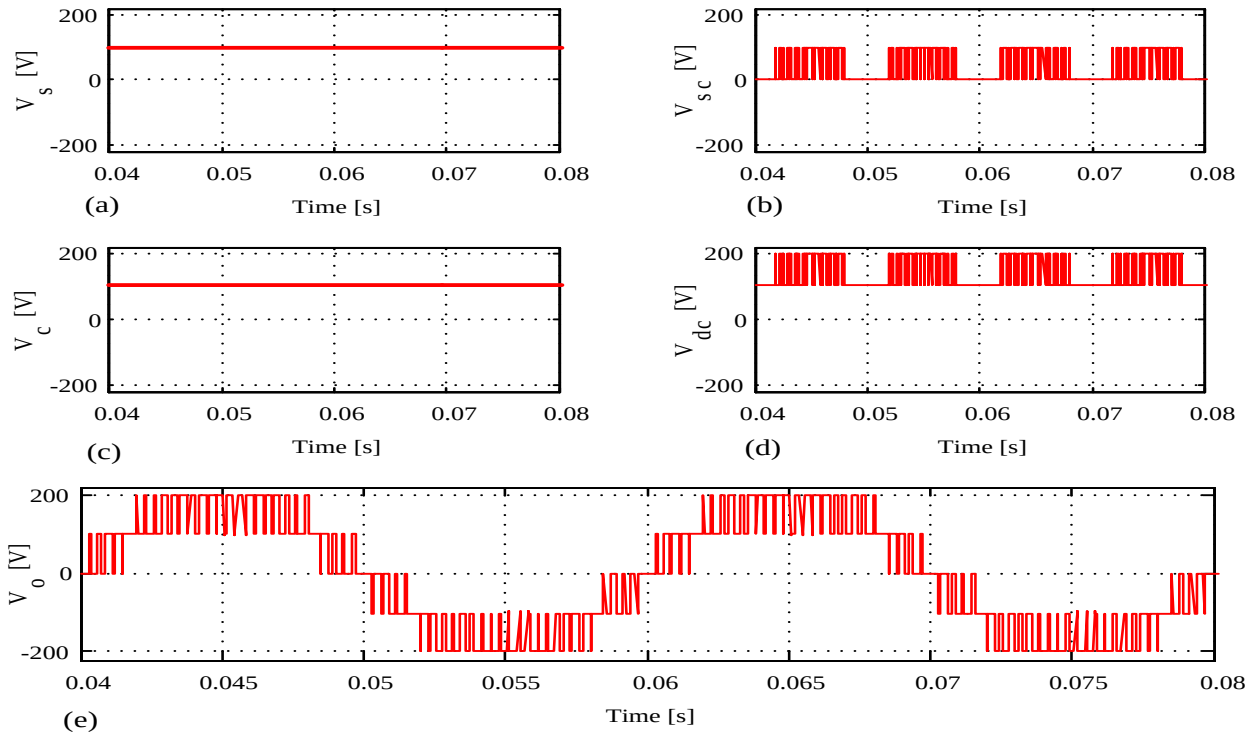

Fig. 10: Simulated five-level inverter voltage waveforms: (a) dc input voltage (b) voltage drop across Sc switch (c) capacitor voltage (d) output dc voltage (e) inverter output voltage.

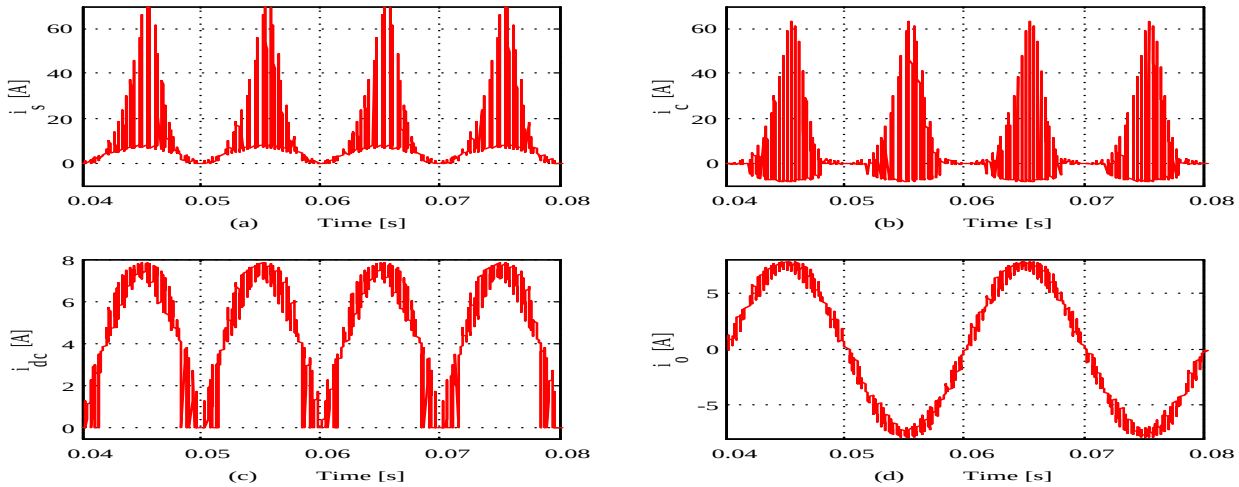

Fig. 11: Simulated five-level inverter current waveforms: (a) dc input current (b) current through Sc switch (c) output dc current (e) inverter output current.

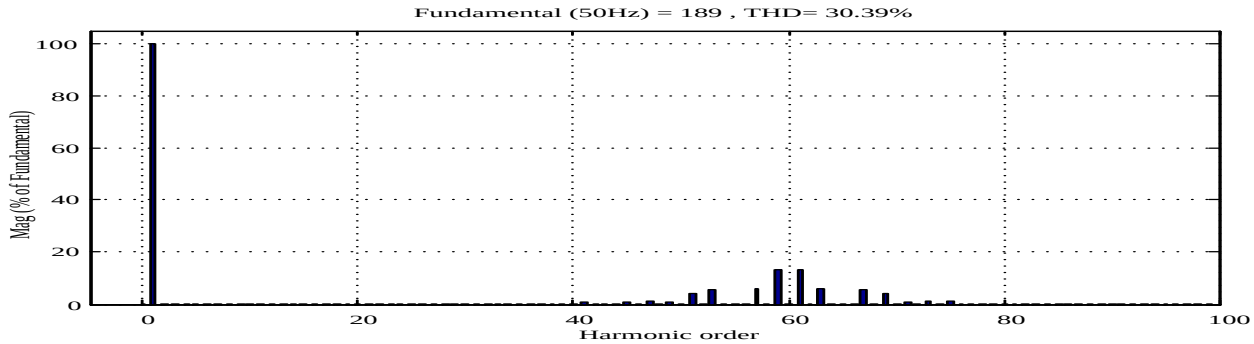

Fig. 12: FFT analysis result of the five-level inverter output voltage

3.1.2 Simulation results based on three-level Output Voltage

In the modulation scheme depicted in Fig. 13, the reference signal, Vref is compared with the carrier signal V_{cr1} to generate the firing pulse for switches S_3 and S2. In this operation the charging switch Sc firing signal remains constantly high. Contrarily, the discharging switch Sd firing signal remains constantly low. It is observed that this operation makes use of only one carrier signal, Vcr1. Fig. 14 and Fig. 15 show the simulated three level voltage and current waveforms for modulation index of 0.95. The spectral analyze result of this synthesized inverter output waveform in Fig. 14 (e) is displayed in Fig. 16. Therein, THD value of 58.24% is achieved in three-level output voltage waveform. Table 1 shows, a comparative analysis of the different modulation schemes discuss between the three-level and five-level output voltages. The simulation results are carried out under currents and voltages THDs. It is observed that the five-level has a better performance.

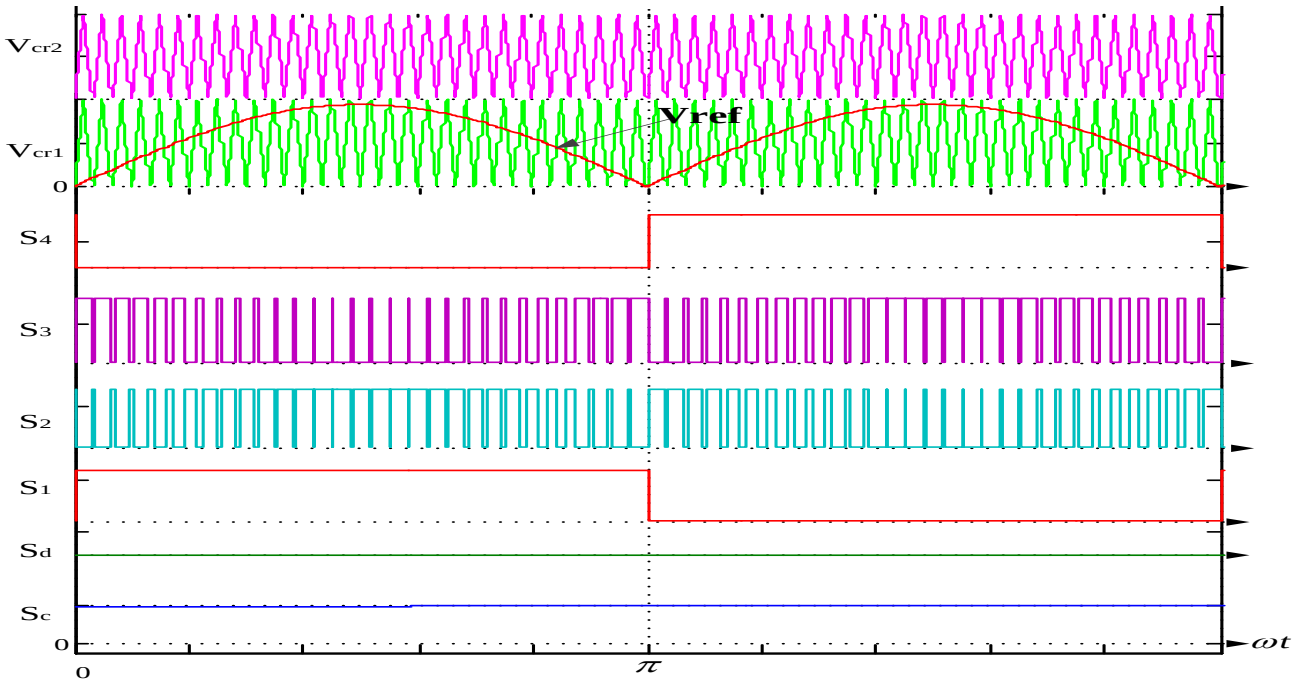

Fig. 13: RRMC SPWM modulation technique for single phase three level inverter.

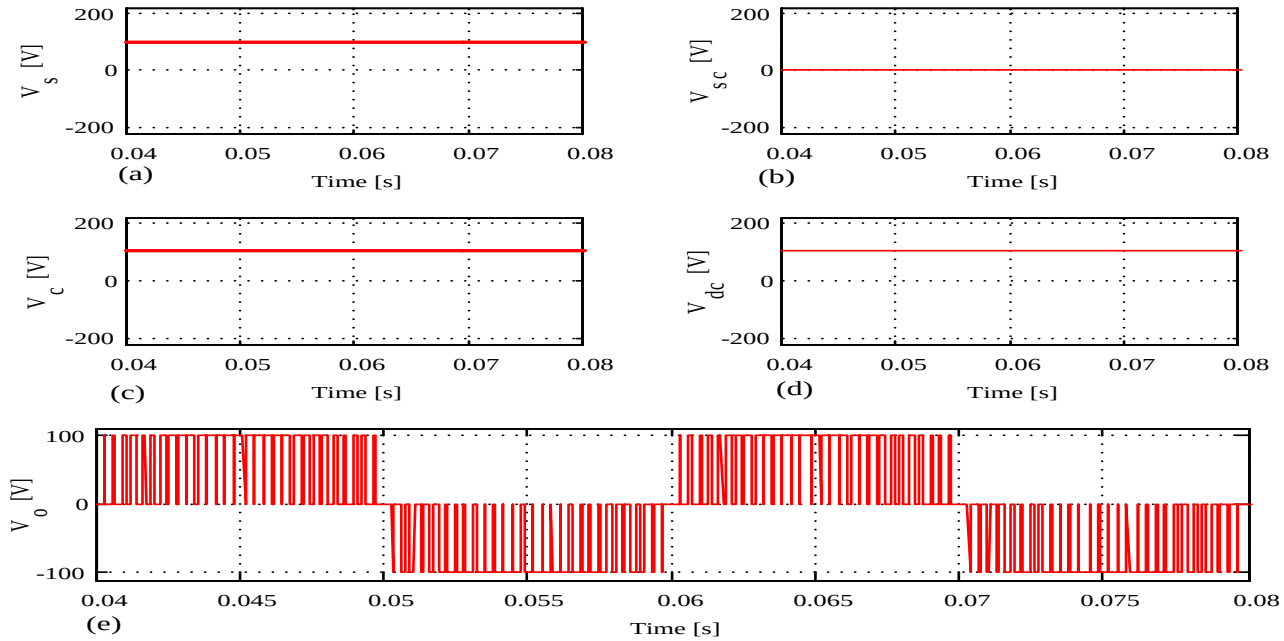

Fig. 14: Simulated three-level inverter voltage waveforms: (a) dc input voltage (b) voltage drop across Sc switch (c) capacitor voltage (d) output dc voltage (e) inverter output voltage.

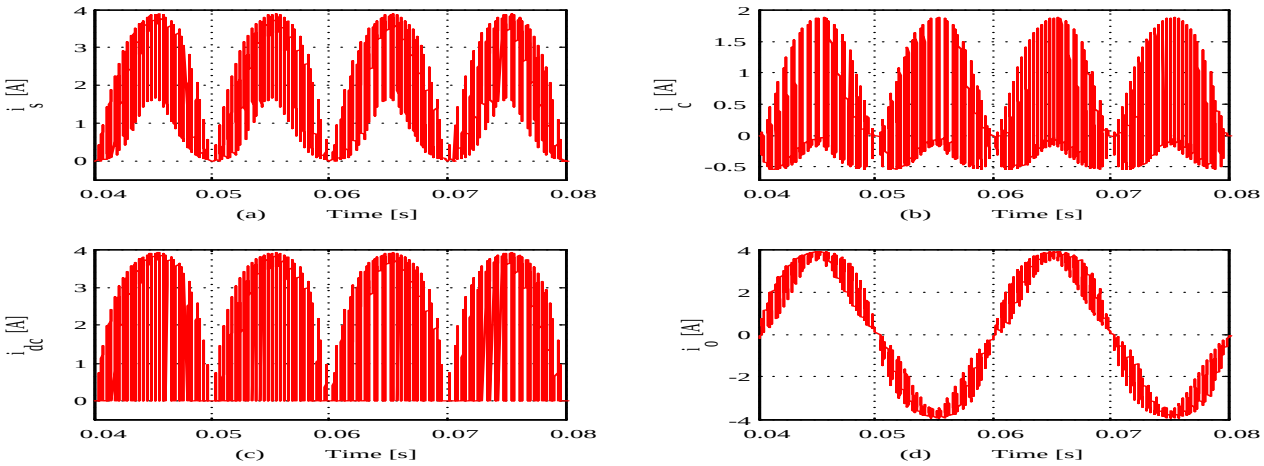

Fig. 15: Simulated three-level inverter current waveforms: (a) dc input current (b) current through Sc switch (c) output dc current (e) inverter output current.

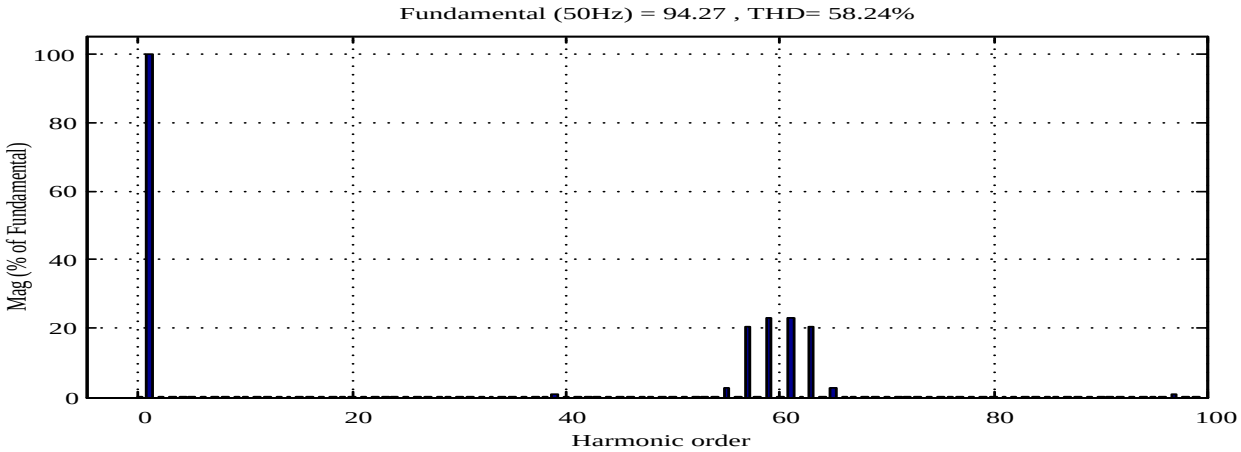

Fig. 16: FFT analysis result of the three-level inverter output voltage

Table 1: Comparison parameters between different modulation schemes

S/No	Modulation scheme (SPWM)	Number of reference signals	Number of carrier signals	Three-Level voltage THD (%)	Three-Level current THD (%)	Five-Level voltage THD (%)	Five-Level current THD (%)
1	RRMC	1	2	58.24	14.58	30.39	7.76
2	PD	1	4	58.29	14.57	30.44	7.75
3	APOD	1	4	58.29	14.57	30.42	7.74
4	POD	1	4	58.24	14.58	30.30	7.73
5	MRSC	2	1	58.24	14.58	30.30	7.73
6	SRMC	1	2	58.29	14.57	30.44	7.75

3.2 Experimental Results

In line with the simulation results, a laboratory prototype was built as shown in Fig. 17. The Figure displays the Oscilloscope, power switch circuit and signal generators. Here, the experimental results are based on the three and five levels output voltages. Figs. 19 – 21 show the experimental switching

signals for the six power switches while Fig. 22 depicts the experimental waveform of the voltage drop across the capacitor and Vdc. The voltage drop across the charging switch is depicted in Fig. 23, while Fig. 24 shows the system output voltage with five-level waveform. The FFT analysis is obtained in Fig. 25.

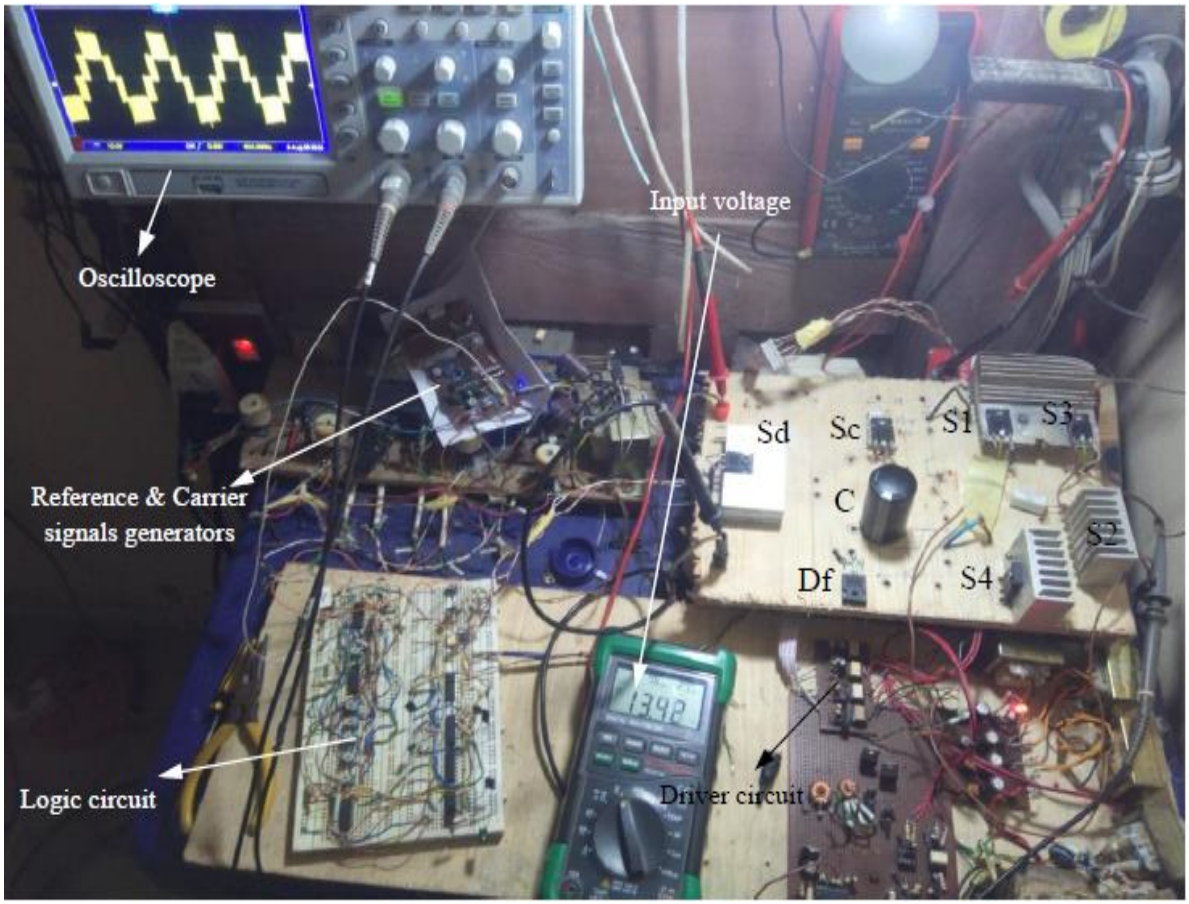

Fig. 17: Experimental prototype of the proposed inverter system.

3.2.1 Experimental results based on five-level output voltage

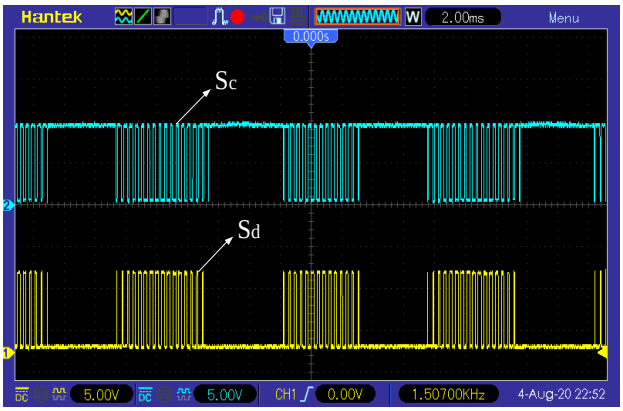

Fig. 19: Experimental waveforms of the gating signal of the dc switches S_c and S_d

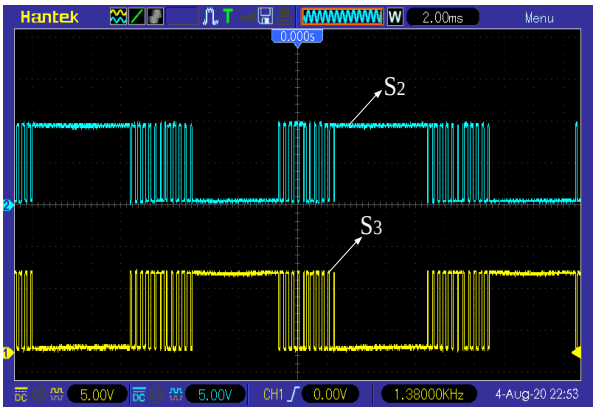

Fig. 20: Experimental waveforms of the gating

signal of the leg-b inverter of switches S_2 and S_3.

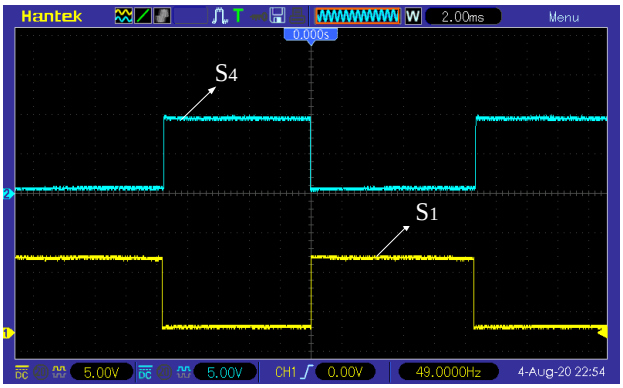

Fig. 21: Experimental waveform of the gating signals of the leg-a inverter of switches S_1 and S_4

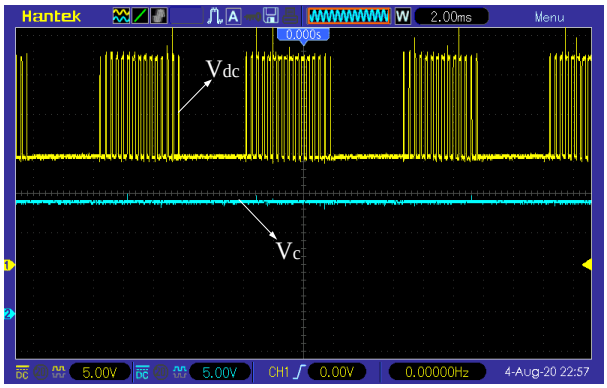

Fig. 22: Experimental waveforms of the voltages drop across capacitor C and V_{dc} voltage.

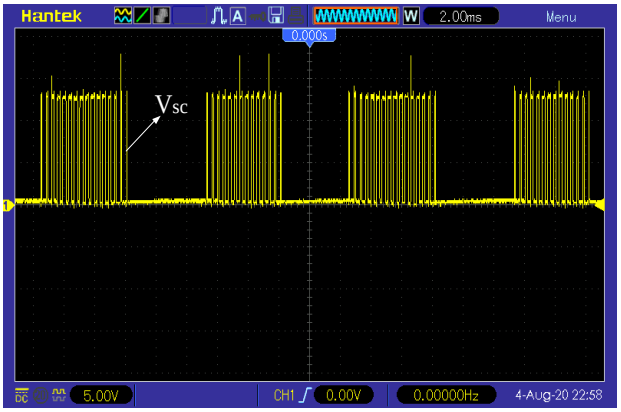

Fig. 23: Experimental waveform of the voltage drop across the charging switch S_c.

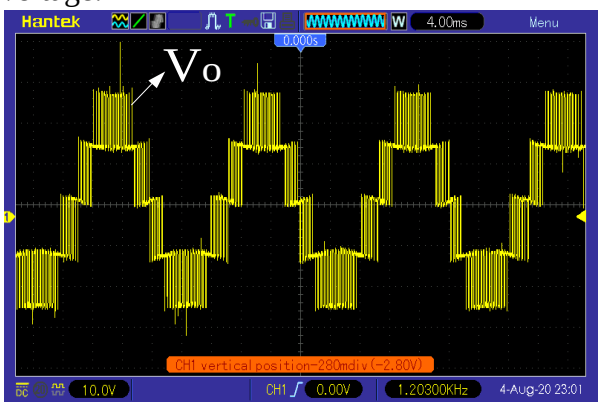

Fig. 24: Experimental waveform of the output voltage, V_o across the load of five level system.

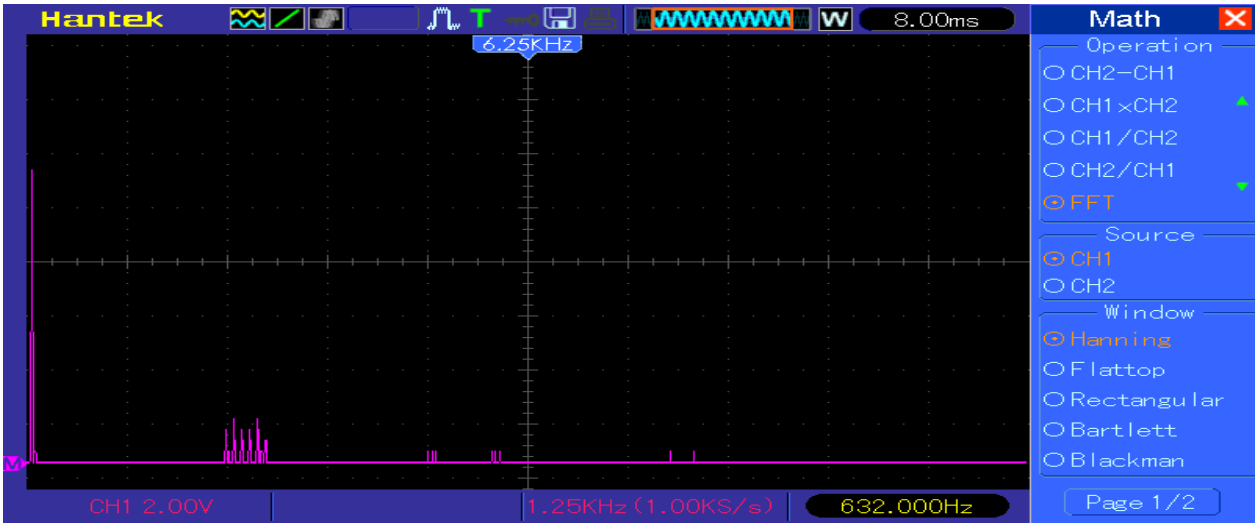

Fig. 25: Harmonic profile of the five-level output voltage

3.2.2 Experimental results based on three-level output voltage

The next part of the experimental results is based on three-level operation, Fig. 26 shows the carrier and reference signals for this operation. Fig. 27 shows the experimental switching signals for power switches S2 and S3. Then, Fig. 28 shows the system output voltage with three-level waveform.

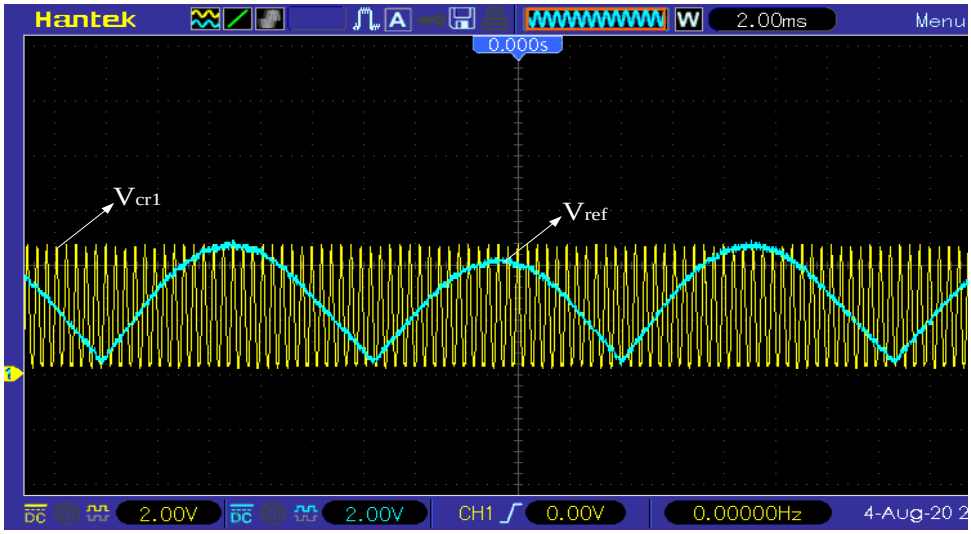

Fig. 26: Experimental waveforms reference and carrier signals.

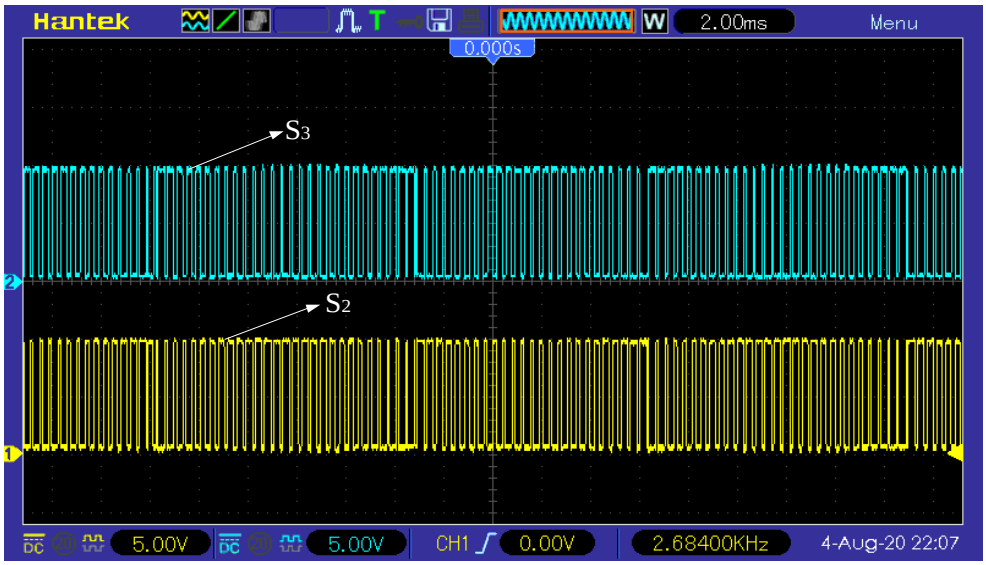

Fig. 27: Experimental waveforms of the leg-b firing signals of switches S_2 and S_3.

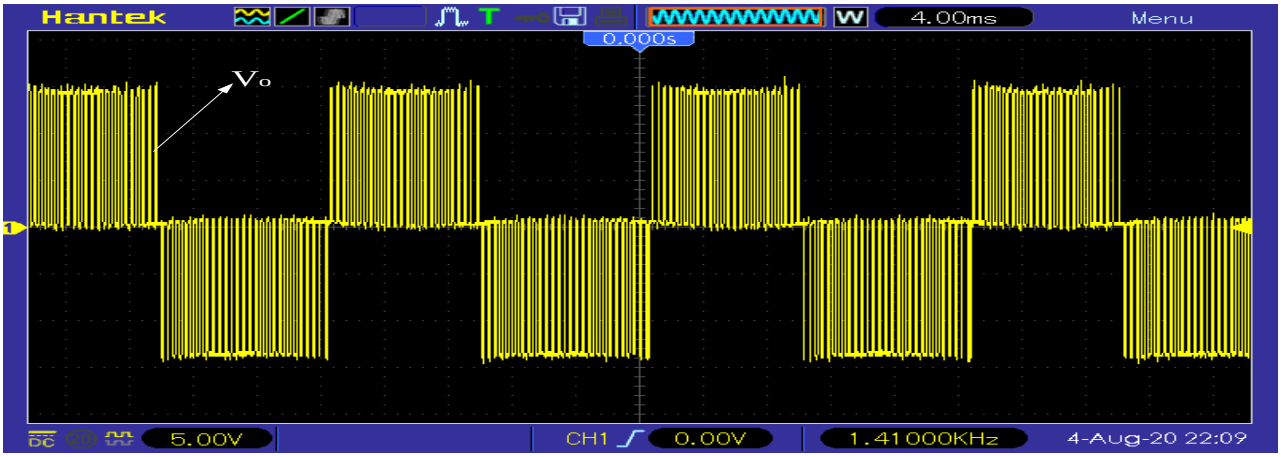

Fig. 28: Experimental waveform of the output voltage, V_o of three level system.

4. Conclusion

Investigating a single-phase, single voltage source multilevel inverter with voltage boosting gain based on different sinusoidal pulse width modulation approach has been presented in this research work. This work showed a novel operation of an inverter circuit capable of generating two different output voltage levels depending on the RRMC SPWM modulation scheme. It is also observed that this modulation technique uses less number of carrier and reference signals for its modulation and generated less harmonic distortion in both output voltage and current. The power circuit configuration and modulation scheme adopted tolerated fault under zero signal at switch Sd. This result is as confirmed in its three-level operation. The waveforms recorded in the implemented section agreed with the simulated part and hence validate the results.

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