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Effect of Temperature on the Quasi Ballistic Transport of a Double Gate Nano-MOSFET

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Abstract

This work analyzes the variation and effect of temperature on the electron transport in a Double Gate Nano-MOSFET (DG MOSFET) using quasi ballistic transport (semi-classical) model. NanoMOS version 4.0.4 is used to simulate and investigate the variation and the effect of temperature covering a range of 50k, 450k, and 850k and its influence on the channel dimension from 0nm to 50nm to obtained electronics properties such as the Average electron velocity, 2D electron density and the Sub-band energy along the channel. The study focuses on the elemental semiconductors (Si and Ge) Channel and compound semiconductors ($GaAs$ and $InAs$) channel under high drain bias than under low drain bias. The result obtained showed that at low temperature for the $Si, Ge, GaAs$ and $InAs$ channels, the 2D electron density was found to be $5.76 \times 10^{11} Cm^{-2}$ with an average electron velocity at a peak value of $6.09 \times 10^{5}\ m/s$ and the Sub-band energy profile along the channels is $-4.98 \times 10^{-1}\ eV$ resulting in high on-state current (I_{on}). At an average temperature for the $Si, Ge, GaAs$ and $InAs$ channels the 2D electron density was found to be $1.75 \times 10^{12} Cm^{-2}$ with average electron velocity at a peak value of $5.76 \times 10^{5}\ m/s$ and the Sub-band energy profile along the channel is $-3.65 \times 10^{-1}\ eV$, while at 850k the 2D electron density was found to be $3.38 \times 10^{12} Cm^{-2}$ with average electron velocity at a peak value of $5.23 \times 10^{5}\ m/s$ and the Sub-band energy profile along the channel is $-1.87 \times 10^{-1}\ eV$ for the $Si, Ge, GaAs$ and $InAs$ channels. The result shows that the average temperature range from 300k to 450k is more appropriate and suitable for digital system design using DG MOSFET.

1. Introduction

The semiconductor industry has made considerable progress, especially regarding the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). MOSFETs have the remarkable feature that as they become smaller they also become cheaper, consume less power, become faster, and enable more functions per unit area of silicon [1, 2, 3]. However, as the density of circuits increases while scaling down there is always an increase in temperature as such the need to study the effect of temperature on MOSFETs [4, 5, 6].

As the physical gate length is reduced and scaled down to feature sizes in the order of atomic dimensions, fundamental limits are approached causing transistors and wires to behave in a manner that is far from ideal [7, 8]. Below 65-nm as reported by [9] several device-level challenges arise

such as short channel effects, drain induced barrier lowering (DIBL), punch through, quantum tunneling through the gate, impact ionization, large parametric variations, and an exponential increase in leakage current, loss of control, reliability issues, excessive process variations, self-heating [9, 10]. Another research by Afzal in 2017 reported those effects to occur below the 22-nm scale. All these phenomena degrade the performance and switching characteristics of MOSFET [11]. This results in major concerns for scaling down the feature size of these devices which poses a dramatic challenge to circuit designing and fabrication at the nanoscale [12, 13].

The metal oxide semiconductor field-effect transistors (MOSFETs) demonstrated with gate length below 20nm shows a rapid and aggressive acceleration of scaling beyond the 2001 ITRS projections into the 10nm region, this brought about the importance to explore more ways to enhance future electronic devices for digital system design [14, 15, 16]. In 2018 the effect of temperature on drain current, threshold, trans-conductance, and sub-threshold leakage current of 7nm MOSFET at a temperature ranging from -60 to 20˚C showed a Linear decrease in drain current and threshold voltage with an increase in temperature and at Low temperature, the current of MOSFET raises because of increase in mobility of electrons & holes increased [17].

As MOSFET shrink to nanometer scales, their dimensions begin to approach the wavelength of the electron. The operation of deep-submicron MOSFETs is now entering a regime in which quantum-mechanical effects become noticeable and thus classical physics is no longer sufficient for accurate modeling of operating characteristics [18, 19].

The goal of this research is to employ a semi-classical model (where some part of the system is treated quantum mechanically) to explore the effect of temperature as the physical channel length of the double-gate MOSFET is varied accordingly from 10nm to 50nm in the interval of 10nm covering a temperature range of 50K, 450K, and 850K. And since the limitations of some materials for high-temperature electronics have led to the search for suitable materials that operate reliably at high temperatures; we study the effect of temperature for a single compound ($Si\ and\ Ge$) and binary compound ($GaAs, and\ InAs$) semiconductors.

1.2 Transport Model

Natori's theory [20] of ballistic MOSFETs highlights the importance of the source to channel barrier [21]. An expression for the strong inversion drain current in the ballistic limit is readily derived as described in Equation (2) [21, 11];

$$I_D = WC_{OX}(V_{GS} - V_T)\widetilde{v_T}\left[\frac{1 - \frac{\mathcal{F}_{1/2}\left(\eta_{F1} - \frac{qV_{DS}}{k_BT}\right)}{\mathcal{F}_{1/2}(\eta_{F1})}}{1 + \frac{\mathcal{F}_0\left(\eta_{F1} - \frac{qV_{DS}}{k_BT}\right)}{\mathcal{F}_0(\eta_{F1})}}\right] \quad (1)$$

Where $V_{GS}\ is$ the gate to source voltage, W is the width of the channel, C_{ox} is the gate oxide capacitance. In analyzing Equation 2 the following Fermi-Dirac integrals are used;

$$\mathcal{F}_{1/2}\left(\eta_{F1} - \frac{qV_{DS}}{k_BT}\right) = e^{\eta_{F1} - \frac{qV_{DS}}{k_BT}} \quad (2)$$

$$\mathcal{F}_0\left(\eta_{F1} - \frac{qV_{DS}}{k_BT}\right) = \ln\left(1 + e^{\eta_{F1} - \frac{qV_{DS}}{k_BT}}\right) \quad (3)$$

At a region above the threshold, the Fermi-Dirac integrals in Equation (1) can also be used to analyze the drain current per micron of width in terms of the ballistic efficiency (B) and can also be simplified to exponential terms where the Sub-band potential at the drain side is lower by qV_{DS}such that $\eta_{F2} - \eta_{F1} = -{qV_{DS}}/{K_B\ \mathrm{T}}$ hence Equation (1) becomes;

$$\frac{I_D}{W} = BC_{OX}(V_{GS} - V_T)\widetilde{v_T}\left[\frac{1 - e^{{qV_{DS}}/{K_B\ \mathrm{T}}}}{1 + e^{{qV_{DS}}/{K_B\ \mathrm{T}}}}\right] \quad (4)$$

The unidirectional thermal velocity plays an important role in transport. Under equilibrium, the thermal average velocity of electrons with positive velocities is zero [22, 23]. Below the threshold, we can assume Maxwell Boltzmann statistics and the thermal velocity (v_T) is given by;

$$v_T = \sqrt{2k_B T/\pi m^*} \quad (5)$$

Where the effective mass is m^*, the average carrier velocity at the beginning of the channel is the equilibrium, uni-directional thermal velocity [22, 24]. Assuming that only one sub-band is occupied the thermal injection velocity $(\widetilde{v_T})$ at the top of the barrier is given by

$$\widetilde{v_T} = v_T \left(\frac{\mathcal{F}_{1/2}(\eta_{F1})}{\mathcal{F}_0(\eta_{F1})}\right) \quad (6)$$

The unidirectional thermal velocity in the non-degenerate limit is the same in 1D as in 2D and 3D and $\widetilde{v_T} \cong v_T$ and for degenerate conditions $\widetilde{v_T} > v_T$. Poisson's equation describes the spatial relationship between a certain electron density distribution and the corresponding electric field [25, 26].

$$\nabla^2 \emptyset = -\frac{1}{\epsilon}(p - n + N_D^+ - N_A^-) \quad (7)$$

Where $\emptyset$ is the electric potential, p is the hole density, n is the electron density, N_D^+ is donor Density and N_A^- is the acceptor density [27, 28]. If we are only treating electrons in the absence of holes Poisson's equation is given by;

$$\nabla^2 \emptyset = -\frac{1}{\epsilon}(-n + N_D^+ - N_A^-) \quad (8)$$

The electron density at a certain energy level is defined as the product of the Local Density of State (LDOS) and Fermi distribution at that energy [29, 27].

$$n(E) = D(E)f(E) \quad (9)$$

Where $n(E)$ is the electron density at energy E, $D(E)$ is the local density of state at energy E *and* $f(E)$ fermi distribution of the electron at energy E [27].

2. Methodology

NanoMos is a 2-D simulator for thin body (less than 5 nm) devices. The program uses a Green's function approach and a simple treatment of scattering based on the idea of Büttiker probes. The double gate device geometry permits an efficient mode space approach that dramatically lowers the computational burden and permits its use as a design tool [30]. Also implemented for comparison is a ballistic solution of the Boltzmann transport equation and the drift-diffusion approaches.

2.1 Simulation Procedure

The transport models treat quantum effects in the confinement direction exactly and the names indicate the technique used to account for carrier transport along the channel. The transport model is solved self-consistently with Poisson's equation. Several internal quantities such as sub-band profiles, sub-band electron densities, potential profiles, and I-V information can be obtained from the source code [27].

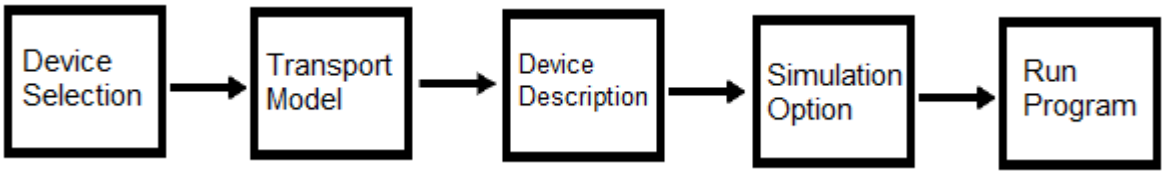

Figure 1: Simulation Procedure

The simulation for the variation in temperature is done using the following procedure;

- The device is modeled by selecting device type (Double gate MOSFET)

- Selecting Transport Model for the device geometry (ballistic transport using semiclassical Approach) and input bias parameters are inputted.
- Devices description parameters are selected.
- Simulation options are inputted (vertical and Horizontal Nodes spacing, convergence parameters, and Number of subbands).
- The program is run to obtain results.

Table 1 gives the initial parameters for the input parameters while the temperature is varied at 50k, 450k, and 850k each temperature result is obtained for a different channel length of 10nm, 20nm, 30nm, 40nm, and 50nm respectively. The source voltage is varied from 0.50V to 1.50V with a step size of 0.10V for $Si, Ge, GaAs, and\ InAs$. The DG-MOSFET is simulated using the parameters in Table 1 to obtain the average electron velocity of the first, second, and third valleys, the 2D electron density, and the sub-band energy profile along the channel for quasi ballistic transport model. The values are obtained at 50k, 250k, and 450k under high drain bias than under low drain bias, and the on-state current in strong inversion is limited by a small portion of the channel near the source, that is the top region of the sub-band potential barrier.

Table 1: Input Parameters for DG-MOSFET simulation

Input Parameters	**Initial Parameters**
V_{GS} (Gate/source Voltage)	0.5
V_{DS} (Drain/source Voltage	0.5
Source/drain doping concentration (N_D)	1.00E+18
Channel body acceptor impurity concentration (NA)	1.00E+12
Top/bottom Gate length	5nm
Channel (film) thickness (T_{ch})	3nm
Top/bottom oxide insulator thickness (T_{OX})	1nm
Top/bottom gate contact work function	4.188ev
Top/bottom insulator relative dielectric constant	3.9
Channel body relative dielectric constant	11.7

3. Results and Discussion

3.1 Average Electron Velocity

The average electron velocities are obtained for $Si, Ge, GaAs, and\ InAs$ at a temperature range of 50k, 450k and, 850k under high and low drain bias**.** The average electron velocity at 50k, 450k, and 850k are shown in Figure 2, 3, 4 and 5 for both Si, Ge, $GaAs$, and $InAs$ respectively. At 50k the average electron velocity is at the peak value of $6.09 \times 10^5\ m/s$ at 50nm, $5.76 \times 10^5\ m/s$ at 450k and $5.23 \times 10^5\ m/s$ at 850k for both Si, Ge, $GaAs$, and $InAs$. It is found that the average electron velocity always increase as the channel length increases. This is because, at the third valley of electrons, the electrons are closer to the conduction band, and thus as the gate voltage $V_{GS} = 0.6v$ increases, the average electron velocity increases before it becomes relatively constant with the smallest decrement above 47 nm. There is an averagely high on-state current (I_{on}) controlled by how rapidly the electrons are transported from the drain high electric field region to the source low electric field region. This conforms with a similar work by Ooi and King in 2013 which reported that at low temperature the average velocity is at maximum peak value than at high temperature [31].

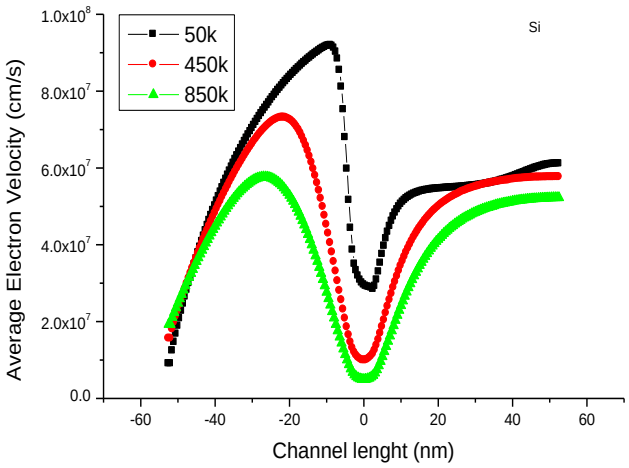

Figure 2: Si Average Electron velocity

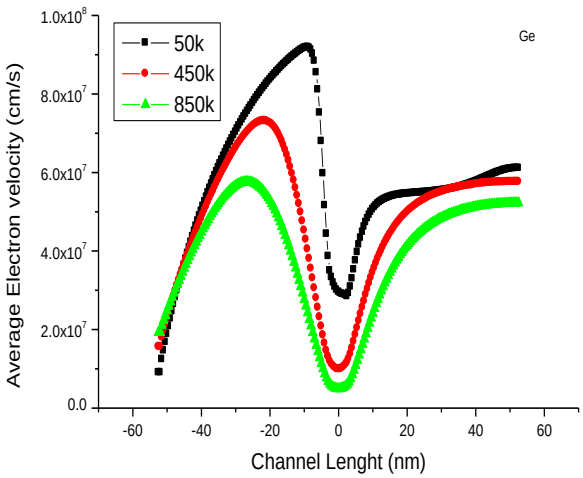

Figure 3: Ge Average Electron velocity

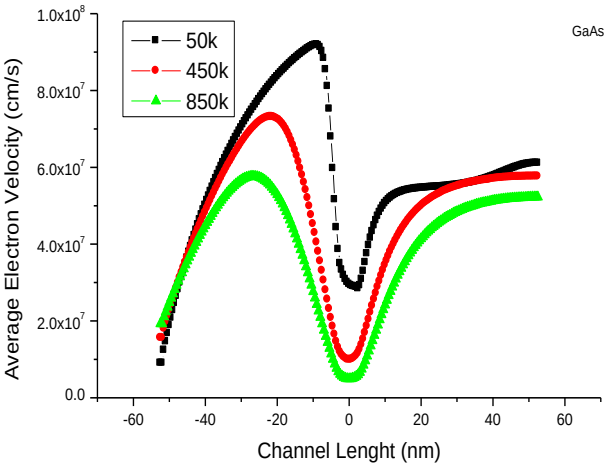

Figure 4: GaAs Average Electron velocity

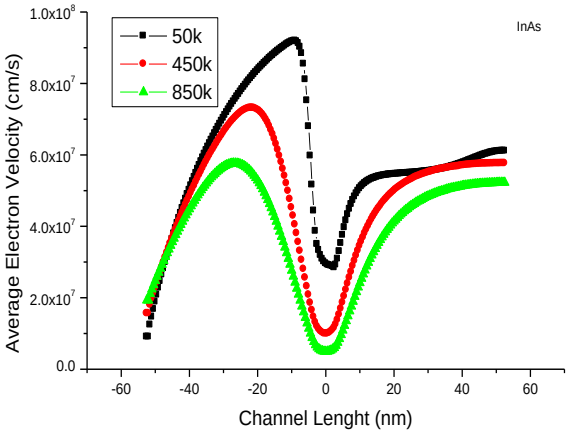

Figure 5: InAs Average Electron velocity

3.1 2D Electron Densities along the Channel

The 2D electron density at 50k along the channel is concentrated from $0.0\,nm$ to around $2.0\,nm$ and reaches its peak value of $5.575 \times 10^{11} cm^{-2}$ at $2.5nm$ for all $Si, Ge, GaAs,$ and $InAs$ as shown in Figures 6,7,8, and 9 respectively. At low temperature, the barrier potential is high resulting in low electron counts, and with gate voltage $V_{GS} = 0.5v,$ the electron density is high from $0.0\,nm\ to\ 2.0\,nm$ to overcome the barrier potential, at $2.5\,nm$. With a step size of $0.1v$ the gate voltage becomes $V_{GS} = 0.6v$ hence the barrier potential is suppressed resulting in a large number of electrons drifting from the drain to the source through the channel region. Thus, at the source region, the electron density was found to be $5.76 \times 10^{11} Cm^{-2}$ at 50k, $1.75 \times 10^{12} Cm^{-2}$ at 450k and $3.38 \times 10^{12} Cm^{-2}$ at 850k. As the channel increases the gate voltage increase with a resulting increase in the potential electron profile which causes rapid decreases in the electrons entering the channel and thus decrease in the electron density at around $12.5nm$ is observed.

At an average temperature, the barrier potential is averagely high which also results in an averagely high electron (Average electron density) at 450K for both $Si, Ge, GaAs,$ and InA. The electron density is at a peak value of $1.75 \times 10^{12} cm^{-2}$ at $0.0\,nm$ and with an averagely high temperature, the barrier is easily suppressed resulting in a large number of electrons drifting from the drain to the source through the channel region. At high temperature, the density of electrons is very high as such

the electrons are concentrated at the lowest channel region ($0.0nm$) with a peak value of $3.383 \times 10^{12} cm^{-2}$ to overcome the barrier potential, but the barrier potential is very low at high temperate so even with gate voltage $V_{GS} = 0.5v$ large number of electrons easily overcome the barrier potential and drift from the drain to source through the channel region before it becomes relatively constant as the channel length increases above $12.5nm$. This behavior is also reported by Rahman et al. in 2003 that the device exhibit a strong drain electron injection and the MOSFET is under the on-state condition because a high drain bias lowers the energy in the drain and a high gate voltage lower the potential energy barrier, which allowed electrons to flow from source to drain [32].

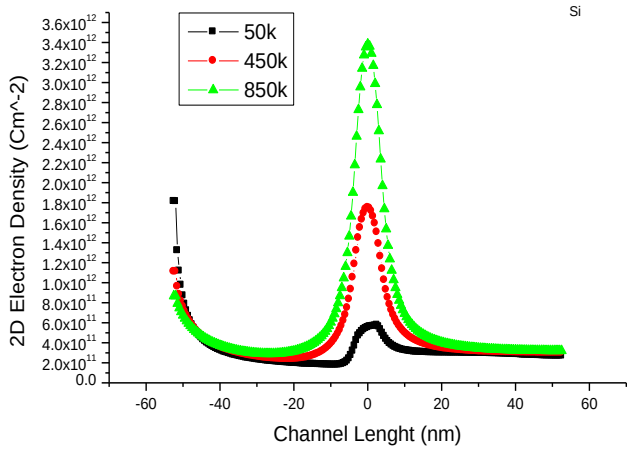

Figure 6: Si 2D Electron density

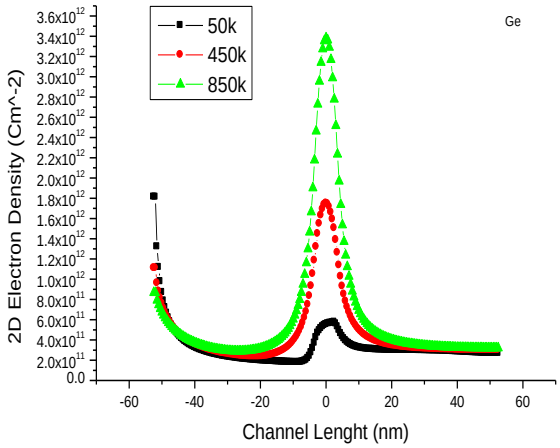

Figure 7:Ge 2D Electron density

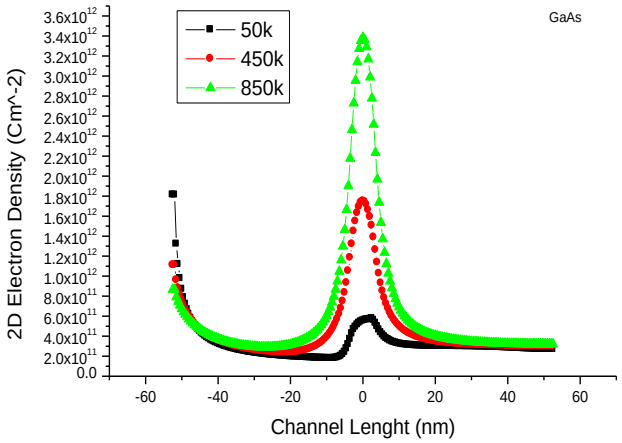

Figure 8: GaAs 2D Electron density

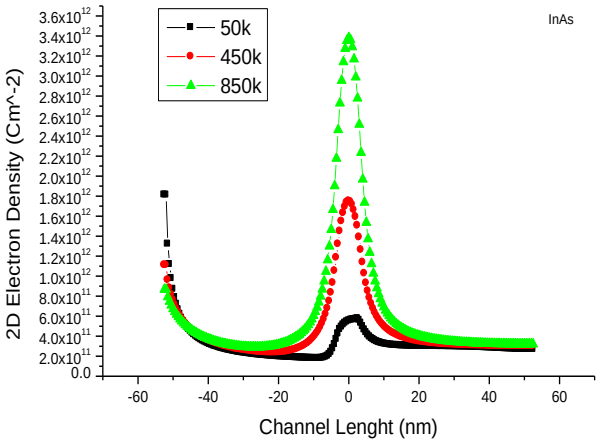

Figure 9: InAs 2D Electron density

3.3 Sub-Band Energy along the Channel

At low gate voltage the energy barrier between the drain and the source along the channel is high this makes the device to be in the off state. When the drain bias is high by a significant increase in the gate voltage the energy is lowered and the high gate voltage lowers the potential energy barrier which allowed electrons to flow from the source to the drain. Figures 10, 11, 12, and 13 show the

first sub-band energy along the channel for both Si, Ge, $GaAs$, and $InAs$ respectively. At low temperature $(50k)$ the potential barrier is very high and the energy along the channel is -4.98×10^{-1} hence the channel is populated with electrons (high electron density) as described in Figure 14, 15, 16, and 17 for Si, Ge, $GaAs$, and $InAs$ respectively. And as the gate voltage increase from $V_{GS} = 0.5v$ to $V_{GS} = 1.5v$ the channel length increases. The energy also increases to overcome the barrier potential and the device is in the on-current state (I_{on}). As the temperature increases to an average temperature $(450k)$, the velocity of the electrons increases along the channel, the energy in the sub-band is averagely$-3.65 \times 10^{-1}\ eV$, and this energy increases as the channel length increases with decreases in the electron density. At high temperature $(850k)$ the potential energy barrier is lowered which causes a significant decrease in the electron density as the channel length increases with sub-band energy at -1.87×10^{-1}. This decrease in electron density allowed the electrons to have much high energy to cross through the channel easier from the source to the drain resulting in a lower average velocity as can be seen from the 3rd valley average electron velocity plot in Figures 2,3,4 and 5 for Si, Ge, $GaAs$, and $InAs$ respectively. This is also reported by Ziabari et al. in 2013 that there is a barrier potential region near the source of the channel that always determines the number and amount of electrons entering the channel from the drain [26].

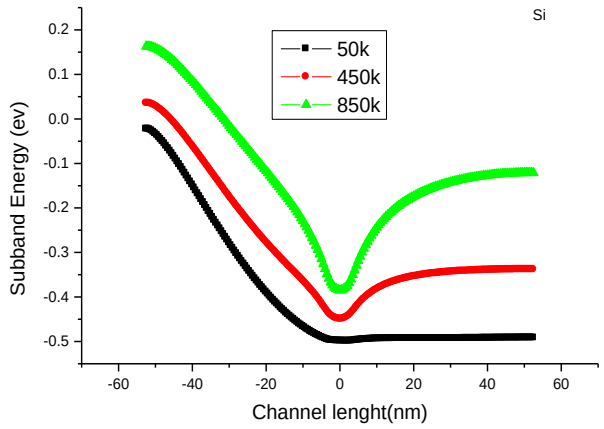

Figure 10: Si sub-band energy

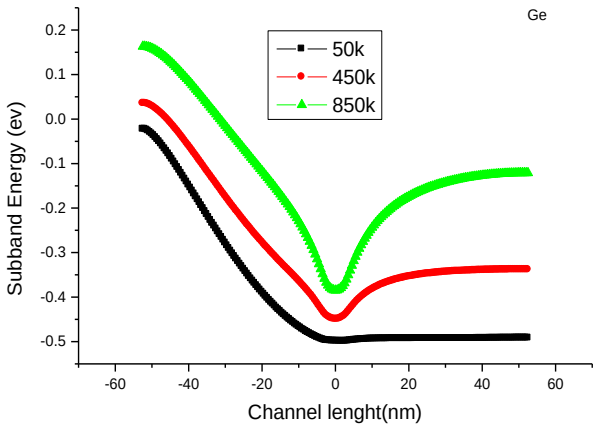

Figure 11: Ge 1st sub-band energy

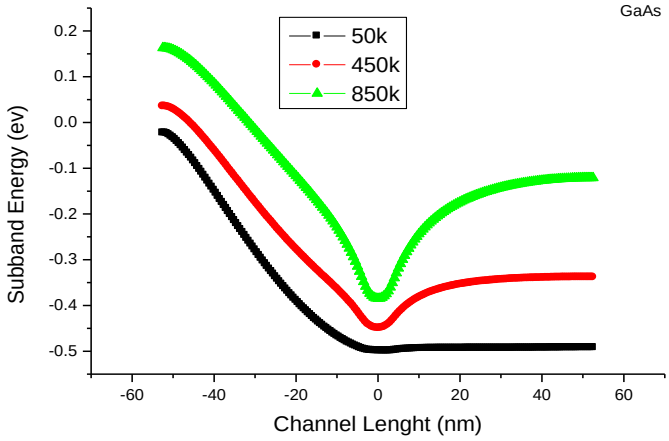

Figure 12: GaAs sub-band energy

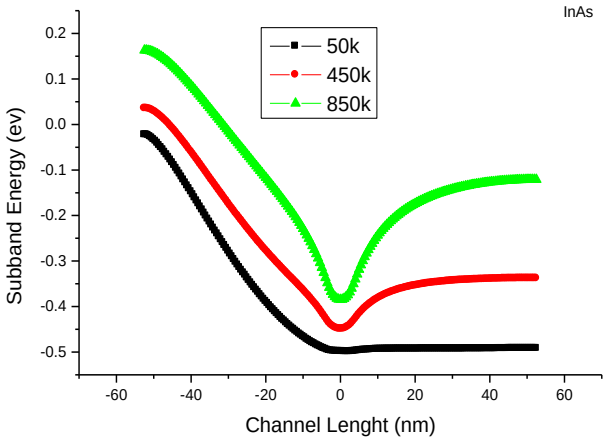

Figure 13: InAs sub-band energy

5.0 Conclusion

The quasi ballistic transport model (semi-classical) is employed in this work using NanoMOS version 4.0.4 simulation software at 50k, 450k, and 850k respectively for Si, Ge, $GaAs$, and $InAs$ semiconductors. The average electron velocity reaches a peak value of $9.02 \times 10^5\ m/s$ at low temperature which is subjected to high barrier potential through the channel region and the energy along the channel is very low hence the channel is populated with electrons (High 2D electron density) at $1.812 \times 10^{12} Cm^{-2}$, thus the electrons need high potential energy to cross over to the source. As the temperature increase from an average to a higher temperature (450k to 850K) the barrier potential reduces and the energy in the sub-band increases with decreases in the electron density. The average electron velocity reduces by averagely high on-state current (I_{on}) controlled by how rapidly the electrons are transported from the drain high electric field region to the source low electric field region. This is true for both the elemental semiconductors (Si, Ge) and the compound semiconductors ($GaAs$ and $InAs$). The results obtained agreed with a similar work by Ooi and King in 2013 that at low temperature the average velocity is at maximum peak value than at high temperature because the semi-classical electrons are treated as particle nature as such the vibration of atoms about their equilibrium position (lattice vibration) increases which hinder the movement of the particulate electrons.

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