Drain Current Characteristics of Carbon-nanotube FET (CNTFET) with SiO_2, ZrO_2 and HfO_2 as Dielectric Materials using FETToy Code

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Article Info

Abstract

Over the last few decades, transistor scaling has taken the centre stage of semiconductor devices. The scaling of metal oxide semiconductor field effect transistor (MOSFET) with SiO_2 thickness has been the driving force towards the technological advancement, but continuous scaling causes a problem of short channel effects, high leakage current, excessive process variation and reliability issues. It is thus, of great necessity to replace the channel material with high mobility materials such as carbon nanotubes FETs to guarantee continued scaling of the device. Carbon Nanotube Field Effect Transistors (CNTFET) are promising Nano-scaled devices for implementing high performance and low power circuits. The Nano device simulator FETtoy was used to assess the electrical characteristics of CNTFETs as channel materials with SiO_2, ZrO_2, and HfO_2 as dielectric materials. Also, effects on temperature variation were investigated. The output parameters that were studied are: drain current, on current (I_{on}), off current (I_{off}), threshold swing (S), drain induced barrier lowering (DIBL), transconductance (g_m), output conductance (g_d), voltage gain (A_v) and carrier injection velocity (v_{inj}). From the results obtained, carbon nanotube as channel material with HfO_2 as dielectric material has higher drain current of $19.3 \mu A$, at higher gate voltage of 0.6 volt and operated near quantum capacitance limit. The obtained results were further compared with other established academic paper published of experimental finding under the same category and are in agreement. This apparently indicate that carbon nanotube as channel material with HfO_2 can be used to increase the performance of carbon nanotube field effect transistor at room temperature with 0.88 gate control parameter to suppress the harmful subthreshold conditions when compared with other MOSFET devices.

1. Introduction

Silicon has been the building block for the progress in the field of electronics until today. However, the scaling limits of silicon are nearing the end since many problems arise as devices become smaller in size. Problems like high-power dissipation, high leakage current, short channel effects (SCEs), excessive process variation, tunnelling effect and reliability issues come into the device and these effects hinder the device performance. It is therefore vital that silicon be replaced by other materials which will take device advancement to a whole new level. New materials with superior electronic, optical, and mechanical properties emerge as a result of the ability to manipulate matter on a nanoscale. Now it is achievable to consider new nano-electronic systems based on new devices with

completely new system architecture, for example: nanotubes, nanowires. Therefore, research on finding new molecular-scale devices with better electrical capabilities to allow device scaling to continue to the atomic level is a major issue in engineering today.

Significant progress has been achieved since the discovery of carbon nanotubes (CNTs) by Iijima in 1991, for both understanding the elementary properties and exploring potential engineering applications. The possible application for nano electronic devices has been broadly investigated since the demonstration of the first carbon nanotube transistors (CNTFETs). Due to its excellent electrical properties, carbon nanotubes are attractive for nano electronic applications.

Low bias transport can be nearly ballistic across a distance of about several hundred nanometers in nanotube. The conduction and valence bands are symmetric, which is beneficial for complementary applications. The band structure is direct, which enables optical emission, and finally, CNTs are highly resistant to electro migration. Noteworthy efforts have been dedicated to comprehend how a carbon nanotube transistor operates and to improve the transistor performance. Most of the up to date CNTFETs operate like non-conventional Schottky barrier transistors [1], [2], which results in quite different device and scaling behaviors from the MOSFET-like transistors [3], [4]. In the near future it is hoped that transistor exceeding the performance of the traditional Silicon MOSFETs can be achieved.

In this work, carbon nanotube as channel material with SiO_2, ZrO_2, and HfO_2 as dielectric materials were analysed and also, the effect on temperature variations using nano electronic device simulating software's (FETtoy) to determine the electrical characteristics. The electrical characteristics considered are; drain current, quantum capacitance, mobile electron, average velocity, transconductance/drain current, quantum capacitance/insulator capacitance, drain induced barrier lowering (DIBL), threshold swing, on – off current, transconductance, output conductance, voltage gain and carrier injection velocity. The most prominent advantages of carbon nanotube field effect transistors over other options for aggressively scaled devices are; very large aspect ratios (length to diameter ratio), typically higher than 1000 and reaching up to 2,500,000, which render their nanostructure quasi-one-dimensional (1D), the room temperature, ballistic transport of charge carries, the reasonable energy gap of $(\sim 0.6 - 0.8eV)$, the demonstrated potential to yield high performance at low operating voltage and scalability to sub-10nm dimension with minimal short channel effect and higher electrical conductivity of about 10^6 to $10^7 S/m$ [5], extremely small, lightweight making excellent replacement for metallic wires, resistant to temperature changes meaning function almost just as well as in extreme cold as they to in extreme heat, and improve conductive mechanical properties of composites

1.2 Carbon nanotube Structure

Carbon nanotubes are formed by rolling graphene sheets like a cylinder. The diameter of the tubes scale to nanometers range (10^{-9}meters) and the length varies from nanometers scale to centimeters scale [6]. These sheets can take up two different forms depending upon the way it is rolled up, i.e. it depends upon the chirality [7]. The Carbon nanotubes has many different structures. These structures differ in length, layer count and thickness. The forms taken up by the nanotubes are metal and semiconductors depending upon the way these sheets are rolled up. The layers of graphene that make up the carbon nanotubes take up the shape of a hexagon, the carbon molecules take up peaks of this hexagonal arrangement. The basic structure of how graphene sheet looks like is shown in Figure 1. These sheets consist of a mesh like structure with a series of carbon atoms. These sheets when rolled up are called carbon nanotubes.
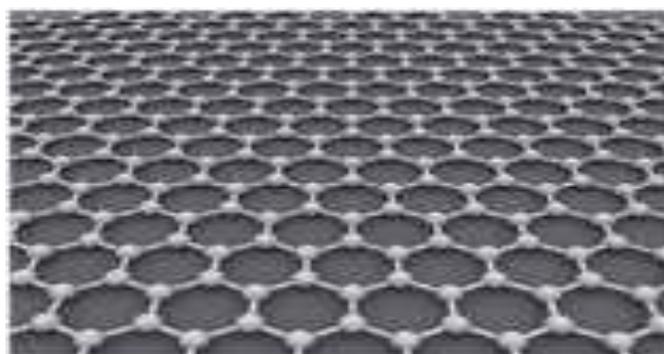
Figure 1. Structure of Graphene [6]

The basic structure of carbon nanotubes is in Figure 2. The structure of carbon nanotubes is basically of two types. The type of nanotubes depends on the shell count that constitutes the tubular structure.
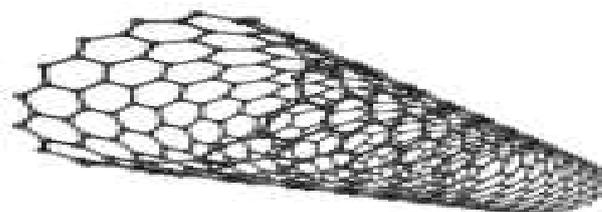
Figure 2. Structure of Carbon nanotube [6]

There are two types of carbon tubes: multi-walled (MWCNTs) and single-walled (SWCNTs). Multi walled Carbon Nanotubes (MWCNTs): This type of carbon nanotubes consists of both the metal and semiconductor layer of cylinder materials. These are arranged in the concentric cylinder pattern. The metallic cylinder contradicts the properties of semiconductor material. Thus, this type of CNTs is usually not preferred for the industry applications [8].

Single walled Carbon Nanotubes (SWCNTs): This type of carbon nanotubes which was discovered in 1993 by [9] which consists of only single layer of grapheme cylinder. A single-well carbon nanotube (SWCNT) can act as either a conductor or a semiconductor, depending on the angle of the atomic arrangement along the tube as shown in Figure 3.
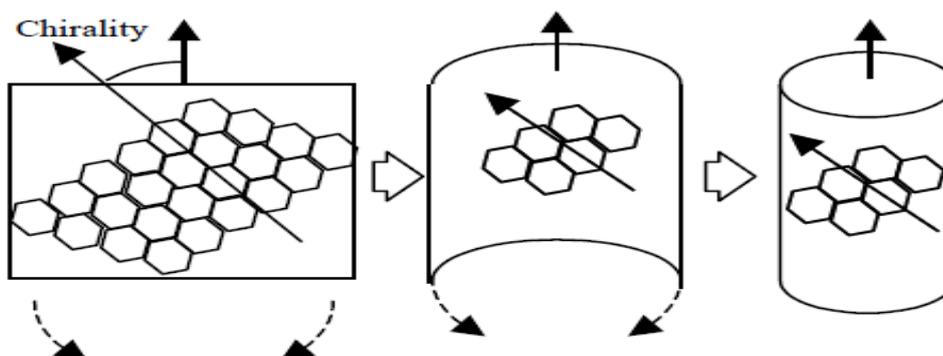
Figure 3. Schematic animations of a carbon nanotube formed by rolling up grapheme and chirality of CNT [10].

which is referred to as the chirality vector and is represented by the integer pair (n, m). A simple method to determine if a CNT is metallic or semiconducting is to consider its indexes (n, m). The nanotube is metallic if $n = m$ or $n - m = 3i$, where i is an integer, otherwise, the tube is semiconducting [10]. The diameter of the CNT can be calculated based on the following equation in [10].

$$D_{CNT} = \frac{C_h}{\pi} = \frac{a\sqrt{m^2+mn+n^2}}{\pi} \tag{1}$$

Where C_h is the length of the chirality vector, $a = 1.42\sqrt{3}\ A^o$
The chiral angle θ is given in [10] by;

$$\theta = \tan^{-1}[\sqrt{3}\,m/(m + 2n)] \tag{2}$$

The threshold voltage of the intrinsic CNT channel can be approximated to the first order as the half bandgap which is an inverse function of the diameter given in [10].

$$V_{th} \approx \frac{E_{gap}}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \tag{3}$$

where a is the interatomic distance between each carbon atom and its neighbor [11]. $V_\pi = 3.033eV$ is the carbon bond energy in the tight bonding model; e is the unit electron charge; The band gap is inversely proportional to the diameter of the carbon nanotube.

$$E_{gap} = \frac{4\hbar v_f}{3D_{CNT}} \tag{4}$$

where v_f is the fermi velocity and D_{CNT} is the diameter of the nanotube [12].
The structure of cylindrical CNTFET is shown in Figure 4. In cylindrical CNTFET, a semiconducting CNT is used as the channel which is surrounded by an oxide layer which is finally surrounded by a metal contact. This metal contact serves as the gate terminal. It was assumed that the metal-nanotube contact resistance and carrier transport through nanotube is ballistic (no scattering). The channel length is an important parameter when fabricating a device. Depending on the types of scattering that take place in the channel, conduction can fall into either the diffusive or ballistic regimes. Because the model used for simulation assumes ballistic conduction, there is no consideration of channel length as there would be no effect so long as ballistic conduction is maintained [10].
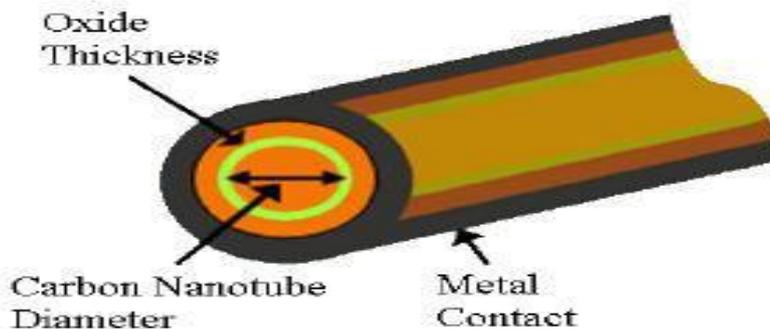
Figure 4. Structure of Cylindrical carbon nanotube [10].

The most important reason behind choosing carbon nanotube is their 1-dimensional characteristic which the carriers are confined on the cylinder of the tube and this gives rise to a strong quantization of electron and hole states and charge transport in 1-D sub band becomes feasible even at room temperature. The reduced phase space for scattering events reduces the probability of back scattering and manifests itself in a high conductivity of carbon nanotubes. By using a single-wall CNT as the channel between two electrodes, like the source and drain contacts of a FET, a coaxial CNTFET can be fabricated. Coaxial devices, due to their geometry allows for better electrostatics since the gate contact wraps all around the channel (CNT) and has a very good control on the transportation of carriers.

1.3 Carbon Nanotube Field Effect Transistor (CNTFET)

A Carbon Nanotube Field Effect Transistors (CNTFET) are promising nano-scaled devices for implementing high performance very dense and low power circuits. A Carbon Nanotube Field Effect Transistor refers to a FET that utilizes a single CNT or an array of CNT's as the channel material instead of bulk silicon in the traditional MOSFET structure [13]. The core of a CNTFET is a carbon nanotube which was discovered by [14] with a typical diameter of 1-20nm they can reach a length of millimeters [15].
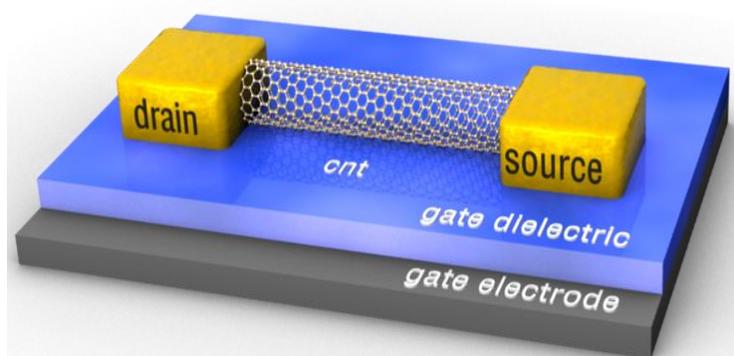
Figure 5. Carbon nanotube FET [13]

CNTFETs were first brought to life in the year of 1998 by Dekker *et al*. Basic principle of operation of CNFET is the same as MOSFET. Electrons are supplied by source and drain collects the electrons. In other words, current flows from drain to source terminal. Gate terminal controls current intensity in the transistor channel and the transistor is in off state if no gate voltage is applied. The main reason that is attracting research on CNTFET is their high channel mobility. The most important reason behind choosing carbon nanotube FETs is their 1-dimensional characteristic; because of which the carriers are confined on the cylinder of the tube and this gives rise to a strong quantization of electron and hole states and charge transport in 1-D sub band becomes feasible even at room temperature. The reduced phase space for scattering events reduces the probability of back scattering and manifests itself in a high conductivity of carbon nanotubes [16]. Secondly, all chemical bonds of the C atoms are satisfied and there is no need for chemical passivation of dangling bonds as in silicon. This implies that CNT electronics would not be bound to use silicon oxide as an insulator. High dielectric constant and crystalline insulators can be used, allowing, among other things, the fabrication of three-dimensional structures. The strong covalent bonding gives the CNTs high mechanical and thermal stability and resistance to electromigration. Their key dimension, their diameter, is controlled by chemistry, not conventional fabrication. In principle, both active devices (transistors) and interconnects can be made out of semiconducting and metallic nanotubes, respectively [17]. By using a single-wall CNT as the channel between two electrodes, like the source

and drain contacts of a FET, a coaxial CNTFET can be fabricated. Coaxial devices, due to their geometry allows for better electrostatics since the gate contact wraps all around the channel (CNT) and has a very good control on the transportation of carriers. The type of Metal-CNT contacts plays crucial role in the output characteristics of the transistor. Heavily doped semiconductors because of the ability to form Ohmic contacts can be used as ideal electrodes but they suffer from high parasitic resistance [18]. Carbon nanotube FETs can be classified into two categories: Back gate CNTFET and Top gate CNTFET

1.3.1. Back gate CNTFET

CNTFET was first demonstrated in 1998 by Tans *et al*. [19] to show a technologically exploitable switching behavior and this work marked the inception of CNFET research progress. In this structure a single SWNT was the bridge between two noble metal electrodes on an oxidized silicon wafer. The silicon oxide substrate can be used as the gate oxide and adding a metal contact on the back makes the semiconducting CNT gate able. Here the SWCNT plays the role of channel and the metal electrodes act as source and drain. The heavily doped silicon wafer itself behaves as the back gate. These CNTFETs behaved as p-type FETs with an I_{on}/I_{off} ratio ~105 [20]. This suffers from some of the limitations like high parasitic contact resistance ($\geq 1M\ ohm$), low drive currents (a few nanoamperes), and low transconductance, $g_m \approx$ 1nS. To reduce these limitations the next generation CNTFET developed which is known as top gate CNTFET.

1.3.2. Top gate CNTFET

To get better performance Wind et al. proposed the first top gate CNTFET in 2003 [20]. In the first step, single-walled carbon nanotubes are solution deposited onto a silicon oxide substrate. Then by using either atomic force microscope or scanning electron microscope the individual nanotubes are located. After which, source and drain contacts are defined and then patterned using high resolution electron beam lithography. High temperature annealing reduces the contact resistance and also increases union between the contacts and CNT. A thin top-gate dielectric is then deposited on top of the nanotube, either via evaporation or atomic layer deposition. Finally, the top gate contact is deposited on the gate dielectric. Arrays of top-gated CNTFETs can be fabricated on the same Silicon wafer, since the gate contacts are electrically isolated from each other, unlike in the back-gated case. Also, due to the thinness of the gate dielectric, a larger electric field can be generated with respect to the nanotube using a lower gate voltage. These advantages mean top-gated devices are generally favored over back-gated CNTFETs, regardless of their more complex fabrication process [21].
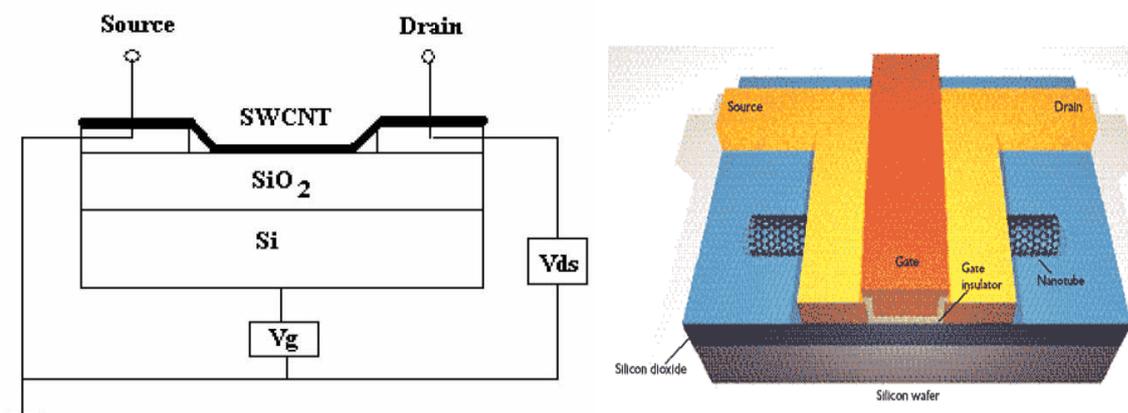
Figure 6. (a) Back gate CNTFET [20],   (b) Top gate CNTFET

The advantages of top gated CNTFET over back gated CNTFET is summarized in Table 1.

Table 1: Comparison between Back gate CNTFET and Top gate CNTFET [20].

Parameters	Back gate CNTFET	Top gate CNTFET
Threshold voltage	-12V	-0.5V
Drain current	Of the order of nanoampere	Of the order of nanoampere
Transconductance	1nS	$3.3\mu S$
I_{on}/I_{off}	10^5	10^6

1.4 MOSFET- like CNTFET

The structure of this device is slightly dissimilar to SB-CNTFET since it uses heavily doped terminals instead of metal. This was formed in order to overcome problems in SB-CNTFET and operates like MOSFET. Unlike SB-CNTFET, source and drain terminals are heavily doped like MOSFET and hence it is called as MOSFET-like CNTFET. This device, as shown in Figure 7, operates on the principle of modulation the barrier height by gate voltage application. The drain current is controlled by number of charges that is induced in the channel by gate terminal. This type of transistor has several advantages over SB-CNTFET. This device is able to suppress ambipolar conduction in SB-CNTFET. It also provides longer channel length limit because the density of metal-induced-gap-states is significantly reduced. Parasitic capacitance between gate and source terminal is greatly reduced and thus allows faster operation of the transistor. Faster operation can be achieved since length between gate and source/drain terminals can be separated by the length of source to drain, which reduces parasitic capacitance and transistor delay metric.

It operates like SB-CNTFET with negative Schottky barrier height during on-state condition and thus it delivers higher on-current than SB-CNTFET. Previous work has shown that this type of device gives higher on-current compared to SB-CNTFET and therefore it can justify the upper limit of CNTFET performance. Based on the device performance, it is obvious that this device can be used to investigate the ballistic transport in CNTFET [22], [23].
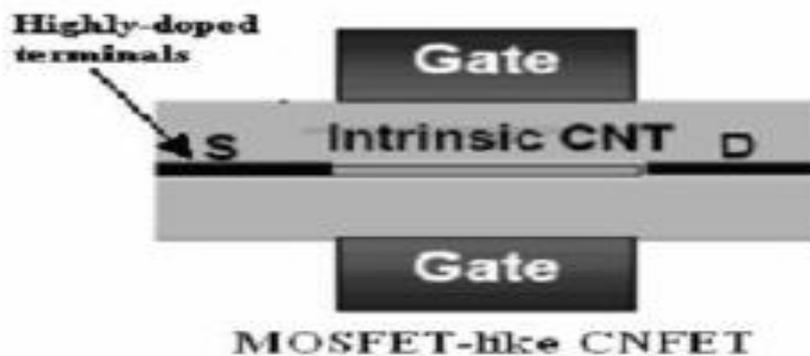
Figure 7. MOSFET- like CNTFET [24]

1.4.1 Carbon Nanotube FET Model

An applied gate voltage (V_g) will induce charge carriers in the nanotube that can contribute to a current passing the nanotube (NT) the induced charge density might not linearly depend on the gate voltage. But the surface potential which corresponds to the Fermi energy in case of nanotubes can be related to the applied voltage. For this reason, the Fermi energy estimated within the CNT when

a gate voltage (V_g) is applied. the number of induced carriers can be calculated from the Fermi energy and finally estimate the conductance G as function of the back–gate voltage V_g.

In analogy to the MOSFET theory where the MOS capacitance is studied at the silicon-oxide of CNT structure. The capacitance $C = dQ/dV$ of this structure is best described by the model of a thin metallic wire at distance d from an infinitely large metallic plate [25].

If the radius of the wire r is much smaller than the distance to the metal plate $r \ll d$, a simple solution can be given for the capacitance per unit length $C_{ox}^* = C_{ox}/L$, this implies that;

$$C_{ox}^* = \frac{2\pi\varepsilon_o\varepsilon_r}{In(\frac{2d}{r}+2)} \tag{5}$$

The nanotube is not surrounded by one single gate dielectric. Between the gate and the nanotube there is SiO_2 with $\varepsilon_{SiO_2} \approx 3.9$, whereas above is air with $\varepsilon_{air} \approx 1$. This as to be considered by an effective dielectric constant $\varepsilon_r^{eff} \sim \frac{\varepsilon_{SiO_2}}{2} \sim 2$ as show in [25]; [26] with an oxide spacing of $d = 400nm$ and a tube radius of $r = 2nm$ to $C_{ox}^* \sim 20pF/m$

1.4.2. Natori's Theory of Ballistic MOSFET

In 1994, Kenji Natori was able to bring up equations that can be used to analyse ballistic nano-transistors. Assuming that a single sub-band is occupied for all categories, the I –V characteristics is as follows:

Two-dimensional double gate, the drain current is given as [27].

$$I_D = WC_{OX}\,v_T\,(V_G - V_T)\frac{(1- e^{-qV_D/k_BT_L})}{(1+ e^{-qV_D/k_BT_L})} \tag{6}$$

Where W is width, V_G is gate voltage, V_D is drain voltage, Cox is oxide capacitance

The drain current of a ballistic MOSFET (under nondegenerate conditions) saturates when $V_D > V_{DSAT} \approx 2(e^{-qV_D/k_BT_L})$. For large drain voltage, the on-current is given by:

$$I_D(on) = WC_{OX}\,v_T\,(V_G - V_T) \tag{7}$$

For small drain voltages, the exponentials can be expanded to find

$$I_D = \left[WC_{OX}\,(V_G - V_T)\frac{v_T}{2(k_BT_L/q)}\right]V_D \;=\; G_{CH}V_D \tag{8}$$

Where
G_{CH} = Channel conductance

$$G_{CH} \;=\; I_D(on)/\,2(k_BT_L/q) \tag{9}$$

$$C_{ins} \;=\; k_{ins}\varepsilon_o/t_{ins} \tag{10}$$

A simple coaxially gated nanowire is assumed, instead of $C_{ins} = k_{ins}\varepsilon_o/t_{ins}$ as for a MOSFET, we have an an insulator capacitance given by [27].

$$C_{ins} = \frac{2\pi k\varepsilon_o}{In\left(\frac{2t_{ins}+t_{wire}}{t_{wire}}\right)} \tag{11}$$

Where t_{wire} is the diameter of the wire
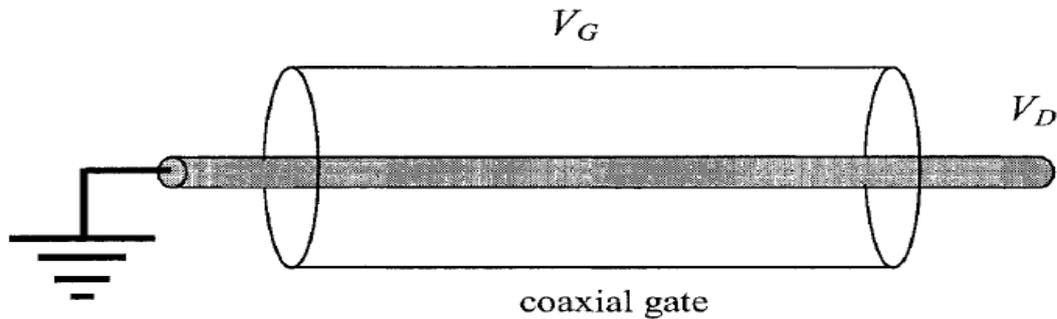
Figure 8. Coaxial gate nanowire [28]

$$I_D = \frac{2q^2}{h} V_D = G_Q V_D \tag{12}$$

So, the channel conductance is just the quantum conductance, as should have been expected. From the perspective of a traditional MOSFET, the linear region current of a MOSFET is

$$I_D = \left(\frac{W}{L}\right) \mu_{eff} C_{ox} (V_G - V_T) = g_d V_D \tag{13}$$

In the quantum capacitance limit where $C_Q << C_{INS}$ the on-current becomes

$$I_D(on) = \frac{2q^2}{h} (V_G - V_T) \tag{14}$$

The transconductance is

$$g_m = \frac{2q^2}{h} = g_d \tag{15}$$

2. Methodology

2.1 Simulation Procedure
The device type selected is carbon nanotube as channel material, silicon as the substrate body, oxide thickness of 0.3nm, initial source fermi level (eV) -0.320, drain control 0.035 and transport effective mass 0.19.

    The simulating procedure was as follows;
1. Modelling of the device was done by choosing the device type (carbon nanotube)

2. Setting the value dielectric material for sets of values (3.9, 15, 25) for SiO_2, ZrO_2, and HfO_2 respectively gate voltage 0-0.6V and drain voltage 0-0.4V at room temperature (300 K) with gate control parameter 0.88, oxide thickness 8nm and diameter of CNT 1.0 nm.
3. The program was then run to obtain results for each set of dielectric material chosen.
4. Setting the value of temperature as (273 K, 300 K, 325 K, 350 K, 375 K) with HfO_2 as dielectric material, gate control parameter 0.88, oxide thickness 8nm and diameter of CNT 1.0 nm.
5. The program was then run to obtain results for each set of temperature chosen.

The results of drain current, quantum capacitance and sub-threshold parameters were obtained and analyzed for different dielectric materials and temperatures. For other parameters fixed and not mentioned see Table A1 in appendix.

3. Results and Discussion

The simulation of carbon nanotube FET as channel material with SiO_2, ZrO_2, and HfO_2 as dielectric materials and temperature variations obtained are; drain current, quantum capacitance, mobile charge, average velocity, transconductance/drain current, quantum capacitance/insulator capacitance, drain induced barrier lowering (DIBL), threshold swing, on – off current, transconductance, output conductance, voltage gain and carrier injection velocity . At low gate voltages, the transistor is in its off state and very little current flows in response to a drain voltage V_d. Beyond a certain gate voltage, called the threshold voltage V_{th}, the transistor is turned on and the ON-current increases with increasing gate voltage V_g.

3.1. Variation of Dielectric Materials
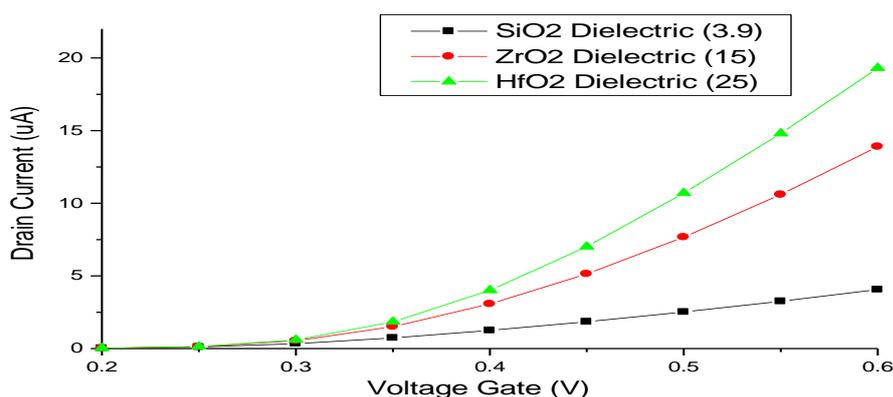
Figure 9: I_d-V_g for different dielectric materials of Carbon nanotube FET
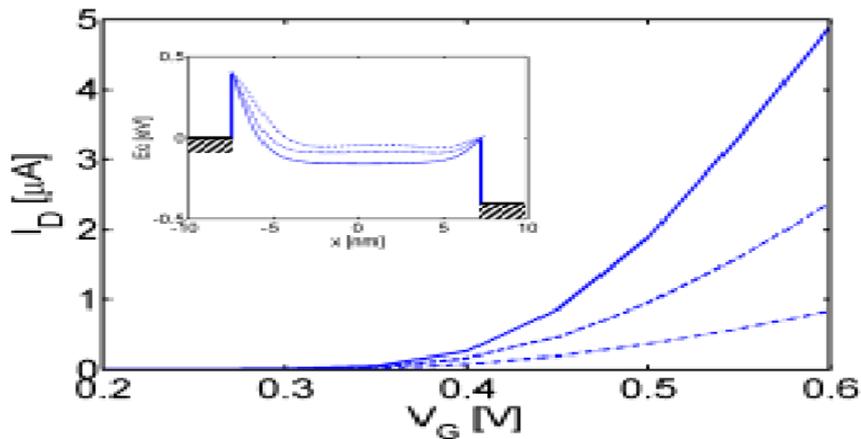
Figure 10: I_d-V_g for different dielectric materials of carbon nanotube FET Experimental by [29] The solid line is for HfO_2 (25), the dashed line for ZrO_2 (15) and the dash-dot line for SiO_2 (3.9)

Figure 9 and 10 displayed the drain current (I_d) characteristics for CNFET and experimental result of CNTFET respectively. From Figure 9, CNTFET with HfO_2 dielectric material curve has higher drain current of 19.3µA and higher threshold voltage around 0.25 volts than SiO_2 and ZrO_2 dielectric materials while Figure 10, shows the experimental results of CNTFET with SiO_2, ZrO_2, and HfO_2 dielectric material by [29], high dielectric materials can provide efficient charge injection to the channel, reduces direct tunneling and provides high gate capacitance. This shows that the simulation of CNTFET with SiO_2, ZrO_2, and HfO_2 are in agreement with that of the experimental finding by Guo *et al*. (2004) because the drain current increases with increase in dielectric material.

3.2. Temperature Variation
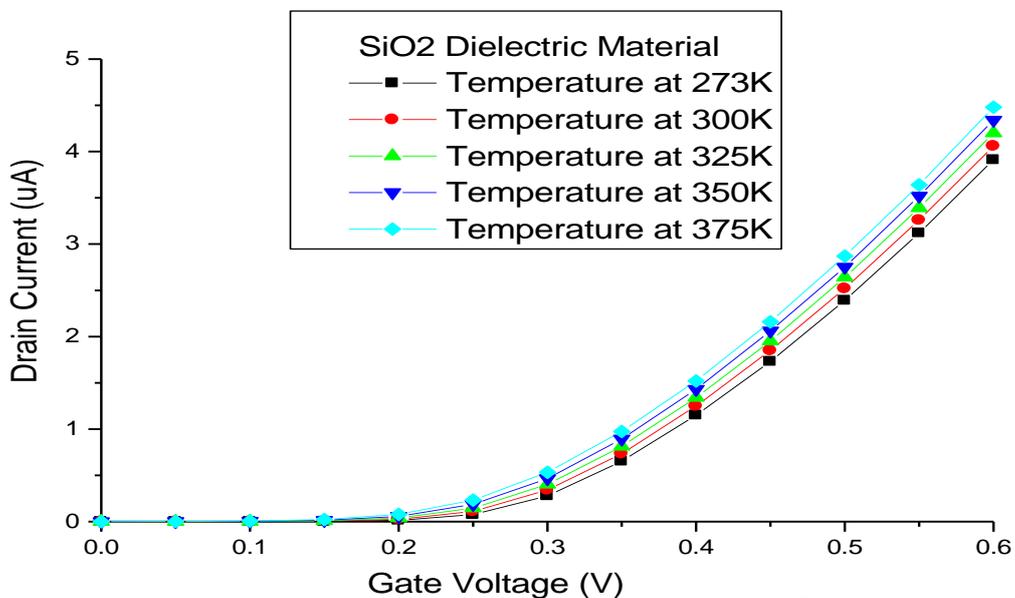
Figure 11: I_d-V_g for different temperature of Carbon nanotube FET with SiO_2 dielectric material
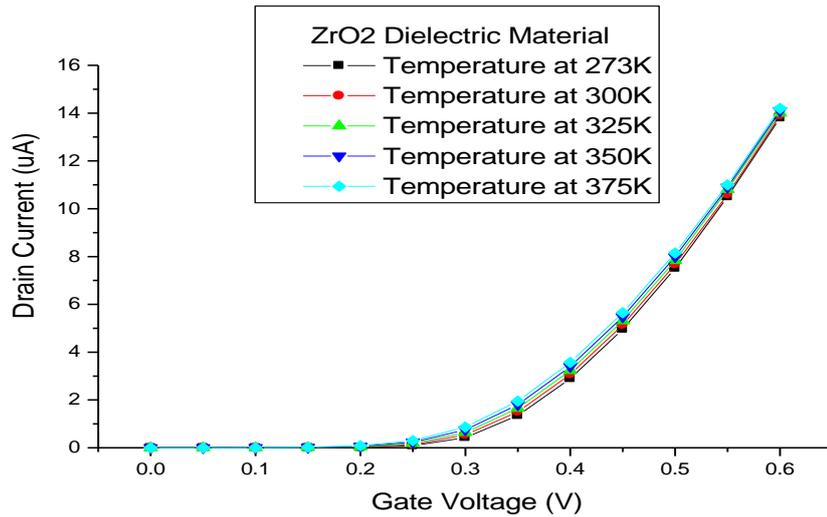
Figure 12: I_d-V_g for different temperature of Carbon nanotube FET with ZrO_2 dielectric material
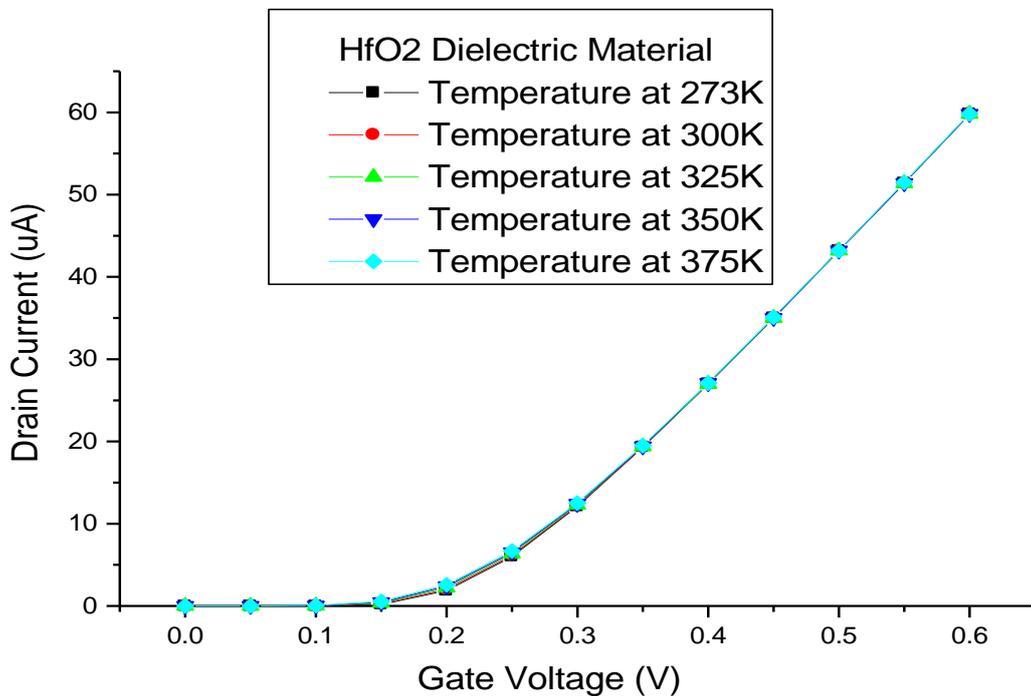
Figure 13: I_d-V_g for different temperature of Carbon nanotube FET with HfO_2 dielectric   material

Figure 11, 12 and 13 displayed the (I_d) characteristics for CNTFET with SiO_2, ZrO_2, and HfO_2 dielectric material at different temperatures. The drain current increases, as the temperature varies with increase in gate voltage. It was observed that with SiO_2 and ZrO_2 dielectric material there is a variation in drain current for change in temperature. While for CNTFET with HfO_2 dielectric material, there is no appreciable variation in drain current for change in temperature. At room temperature, CNTFET with HfO_2 dielectric material has higher drain current $59.8\mu A$ with higher

gate voltage 0.6 volts which is very similar or the same when comparing with other temperature curves.

3.3. Sub-threshold Parameters

The devices sub threshold regions are drain induced barrier lowering (DIBL), threshold swing, on – off current, transconductance, output conductance, voltage gain and carrier injection velocity. Device physics and design equations of carbon nanotube transistors are given in detail in [12]; [30].

3.3.1. Sub-threshold Parameters on Variation of Dielectric Materials

Table 2: Comparison Output of Carbon Nanotube FET with Higher Dielectric Material (HfO_2) at Room Temperature

Output parameters	CNTFET with high dielectric materials by Simulation	CNTFET with high dielectric materials by Experiment finding of Gou et al., (2004)
Carries injection velocity (v_inj) m/s	3.535e+05	3.0e+05
Threshold swing (S) mV/dec	67.71	70
Trans-conductance (gm) S/m	8.943e-05	1.2 e-05
Threshold Voltage (V_{th}) V	0.25	≈ 0.35

Table 3: Output of Carbon Nanotube FET using Different Dielectric Materials at Room Temperature

Output parameters	CNTFET with SiO_2 as dielectric (3.9)	CNTFET with ZrO_2 as dielectric (15)	CNTFET with HfO_2 as dielectric (25)
Ion (A)	4.063e-06	1.392e-05	1.93 e-05
Ioff (A)	2.936e-11	2.936e-11	2.936e-11
Threshold swing (S) mV/dec	67.72	67.71	67.71
DIBL mV/V	65.65	65.65	65.65
Trans conductance (gm) S/m	1.609e-05	6.597e-05	8.943e-05
Output conductance (gd) S/m	6.657e-07	2.744e-06	3.661e-06
Voltage gain at highest gate & drain Bias (Av)	24.18	24.04	24.42
Carries injection velocity (v_inj) m/s	2.251e+05	3.125e+05	3.535e+05
Ion/Ioff ratio	1.38e +05	4.74e +05	6.57e +05

Table 2 shows comparison output of carbon nanotube simulation with higher dielectric material (HfO_2) together with that of experimental finding of Guo *et al.,* (2004) for carries injection velocity, threshold swing, trans-conductance and threshold voltage while Table 3, shows output simulation of carbon nanotube FET of other sub threshold parameter on variation of dielectric materials. The on current(I_{ON}), or drive current in HfO_2, is higher than other dielectric materials, however, since the nanotube has ballistic conductance, it actually has a smaller resistance. Thus, the power consumption is smaller. Increase in dielectric materials leads to increase in threshold swing, transconductance, output conductance, voltage gain, carrier injection velocity, and decrease in

DIBL. In addition, the off current (I_{OFF}) is the same for all dielectric materials which means that the power being wasted while the transistor is off is the same.

4. Conclusion

In this work, the electrical characteristics of carbon nanotube as channel materials with SiO_2, ZrO_2, and HfO_2 dielectric layers were analysed using FETtoy codes. From the results obtained, HfO_2 dielectric layer can be used to increase the performance of carbon nanotube field effect transistor at room temperature with 0.88 gate control parameter. HfO_2 dielectric material has higher drain current of $19.3\mu A$ and operated near quantum capacitance limit. This is in agreement with the experimental finding of Guo *et al*. (2004) with the same dielectric materials, oxide thickness 8nm, higher gate voltage of 0.6V and drain voltage of 0.4V at room temperature.

The effect of different dielectric was scrutinized and was found that drain current increases with increasing in dielectric material. So, by replacing higher dielectric material in the CNTFET as channel material, it is possible to improve the performance. Also, it was observed that I-V characteristics of HfO_2 dielectric material do not vary that much with the change of temperature. Therefore, effect of temperature variation on the performance of CNTFET with HfO_2 dielectric material can be ignored.

Finally, Carbon nanotube-based technology develops the most promising devices among emerging technologies because it has most of the desired features and it is also expected to sustain the transistor scalability while increasing its performance and offer several advantages when compared to silicon-based technology.

Acknowledgment

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Appendix

Table A1: Input Parameters for the Simulation using FETToy

Inputs parameters	Variation in Parameters				
Dielectric materials (k)	SiO_2 (3.9)	ZrO_2 (15)	HfO_2 (25)		
Temperature (T) K	273	300	325	350	375
Diameter of CNT (nm)	1.0	1.0	1.0	1.0	1.0
Gate control parameter (CGP)	0.88	0.88	0.88	0.88	0.88
Initial source Fermi Level (eV)	-0.320	-0.320	-0.320	-0.320	-0.320
Oxide thickness Tox (nm)	8.0	8.0	8.0	8.0	8.0
Drain control	0.035	0.035	0.035	0.035	0.035
Transport effective mass	0.19	0.19	0.19	0.19	0.19